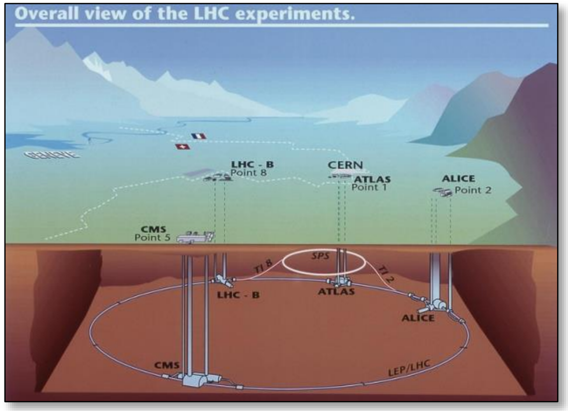
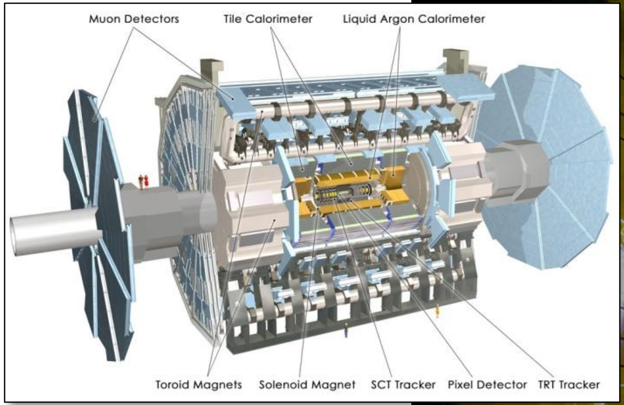
Design analoger Schaltkreise
Vorlesung 1

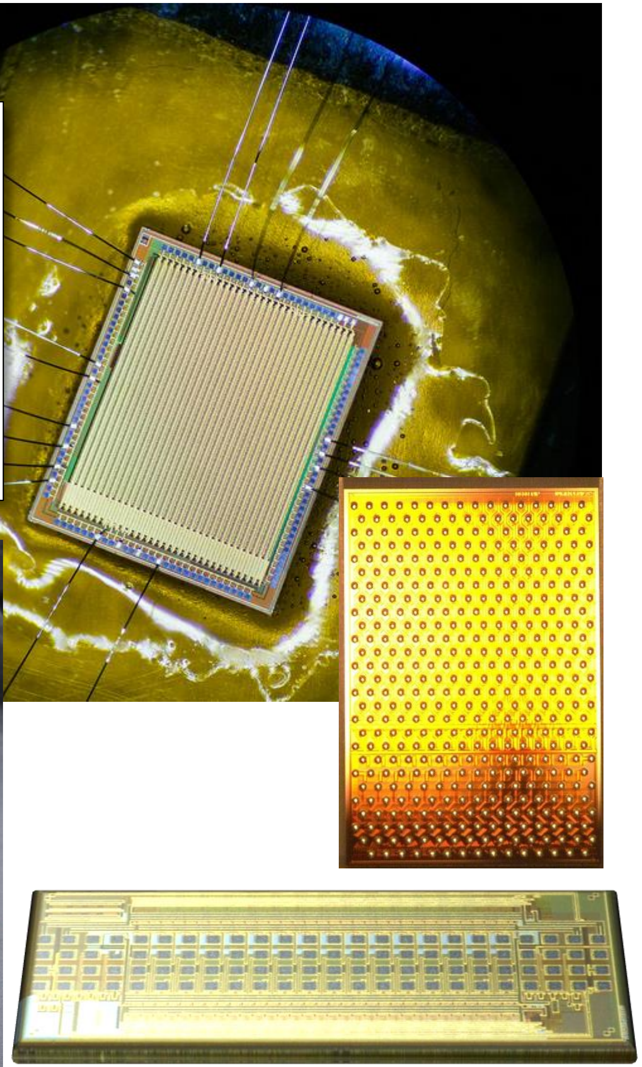
- Institut für Prozessdatenverarbeitung (IPE) am KIT Campus Nord
- ASIC und Detektor Labor
- Detektoren an Teilchenbeschleuniger

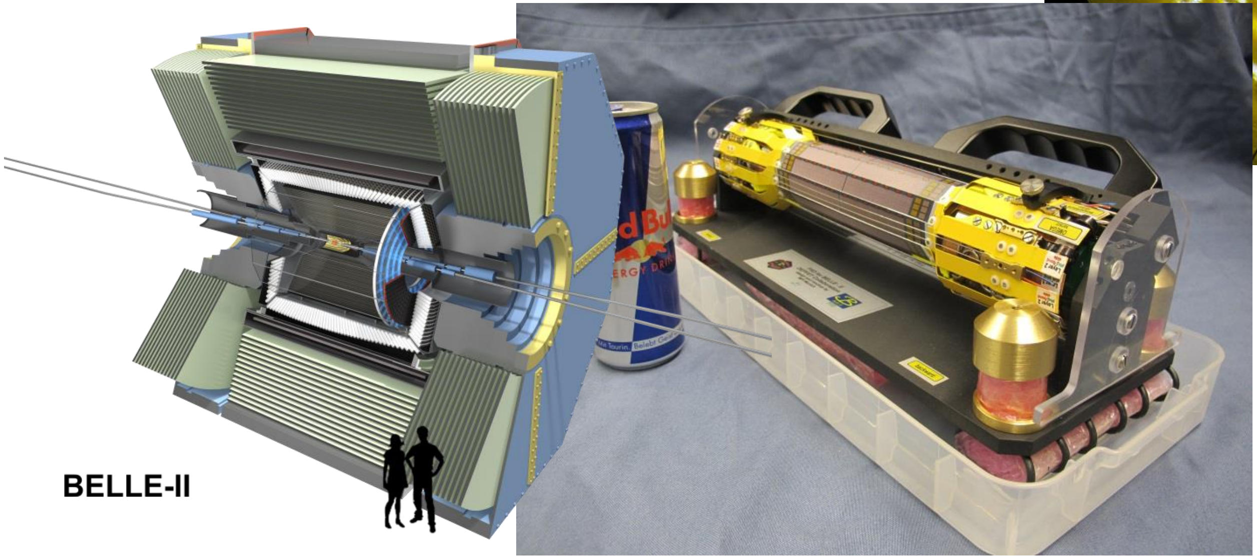
Large Hadron Collider


Overall view of the LHC experiments.
GENEVE
LHC - B Point 8
CERN
ATLAS Point 1
ALICE Point 2
CMS Point 5
SPS
TI 8
TI 2
LHC - B
ATLAS
ALICE
CMS
LEP/LHC

Experiment ATLAS


Muon Detectors
Tile Calorimeter
Liquid Argon Calorimeter
Toroid Magnets
Solenoid Magnet
SCT Tracker
Pixel Detector
TRT Tracker



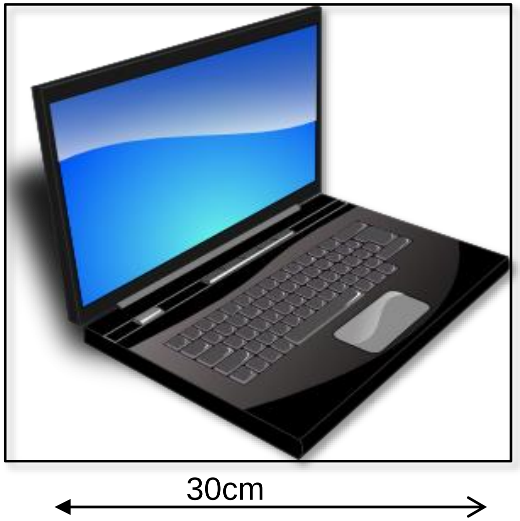


BELLE-II

- Vorlesungen und praktische Übungen mit Chipdesign-Software (CIP-Pool am IMS)
- Übungen ab November
- Kontakt: ivan.peric@kit.edu
- Kontakt: richard.leys@kit.edu
- Inhalt ist neu – neue Skripten bald
- https://www.ims.kit.edu/324_201.php

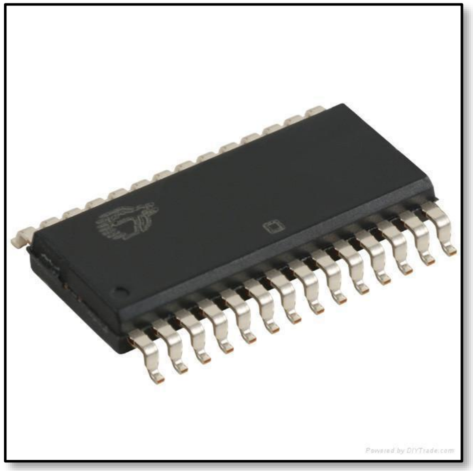
Design analoger Schaltkreise

Electronic device

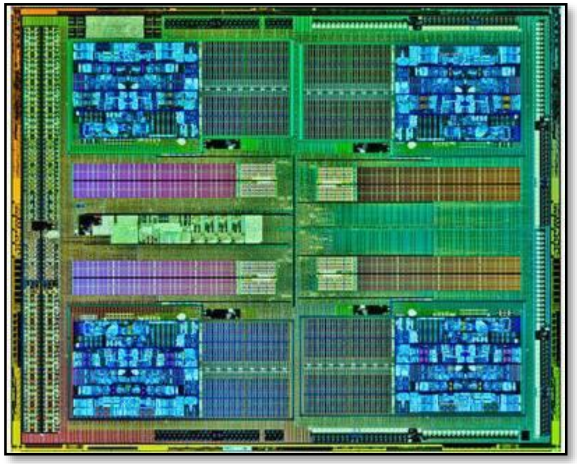


PCB

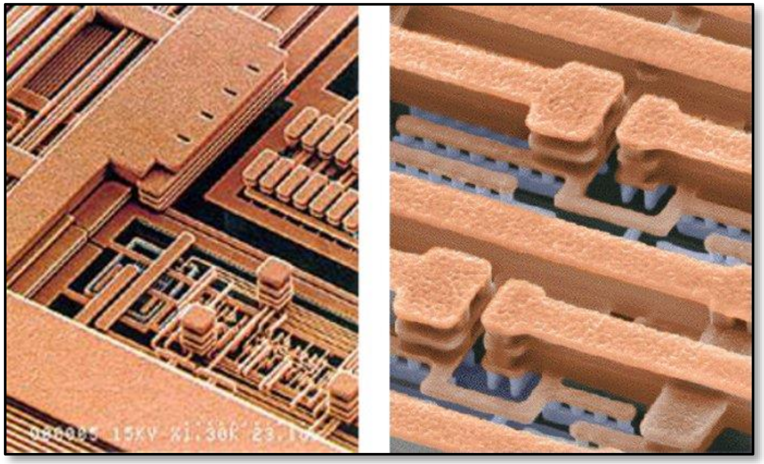
Integrated circuit



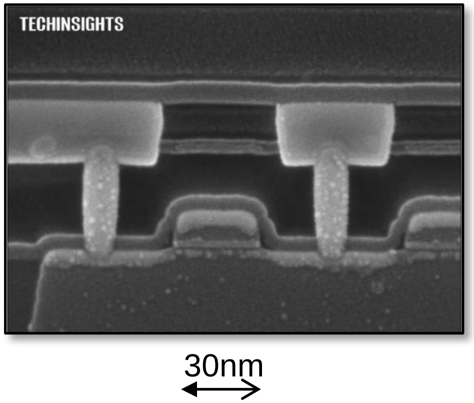
Integrated circuit - core



Interconnection



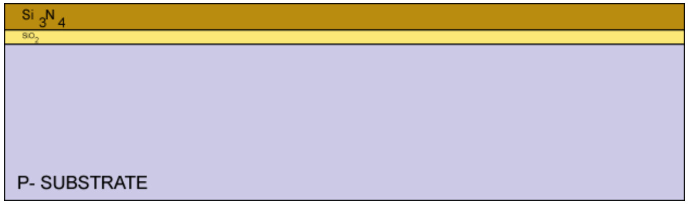
Transistor



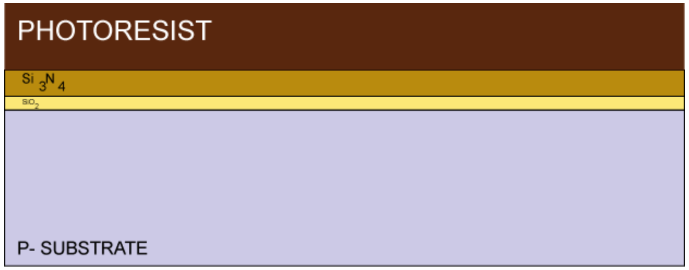
- Vorkenntnisse: Vorlesungen Elektronische Schaltungen und VLSI-Technologie
- MOSFET, JFET, Bipolar-Transistor (BJT)
- Einfache elektronische Schaltungen
- Kleinsignalmodelle, Arbeitspunkt
- Prinzipen der IC Herstellung

- Prinzipen der IC Herstellung
- Wiederholung von Schritten
- Oxid-, Silizium- oder Metalllagen werden auf einem Si-Substrat erzeugt
- Photolithographie (Photolack, UV Licht, trocken- und nassätzen)
- Lagen werden strukturiert
- Silizium wird dotiert
- Link: http://www.halbleiter.org/wie-wird-ein-mikrochip-hergestellt/

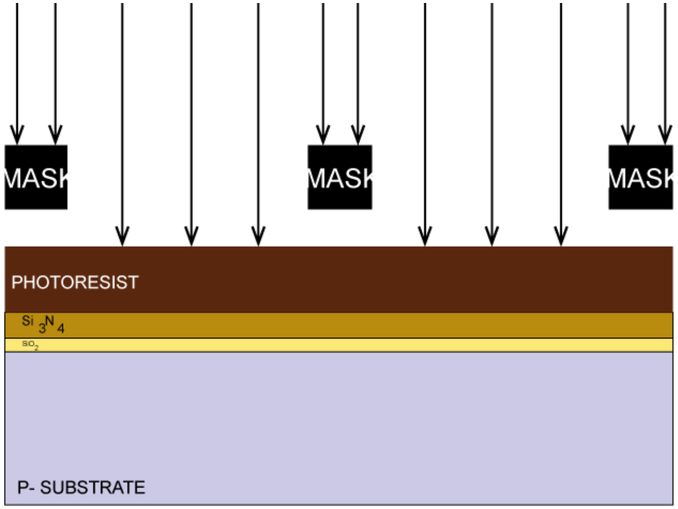
1. Deposition of silicon oxide and nitride


Si_3N_4
SiO_2
P- SUBSTRATE

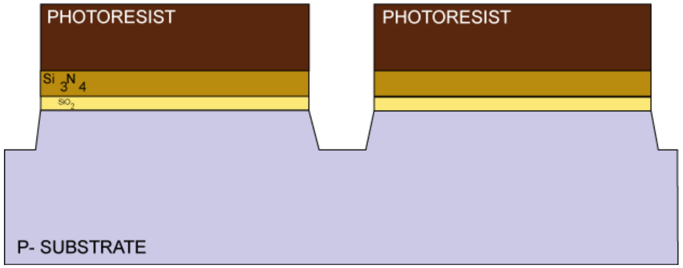
2. Photoresist deposition


PHOTORESIST
Si_3N_4
SiO_2
P- SUBSTRATE

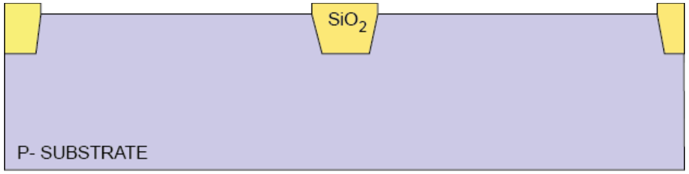
3. Illumination of the photoresist through the mask


MAS
MAS
MAS
PHOTORESIST
Si_3N_4
SiO_2
P- SUBSTRATE

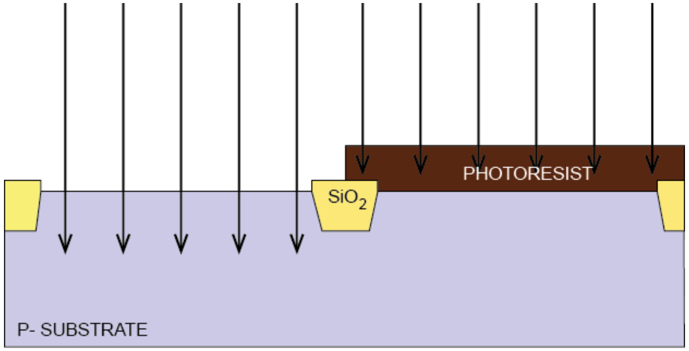
4. Removing illuminated photoresist, etching silicon nitride, etching isolation tranches in silicon


PHOTORESIST
PHOTORESIST
Si_3N_4
SiO_2
P- SUBSTRATE

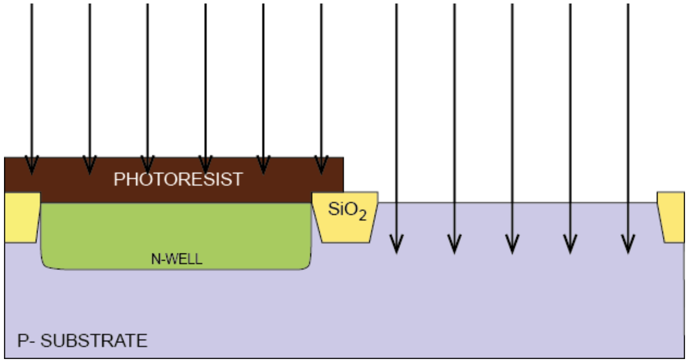
5. Filling isolation trenches with SiO2


SiO_2
P- SUBSTRATE

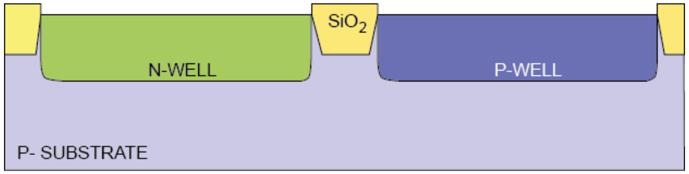
6. Ion implantation (Phosphor ~100 keV) -> N-well formation


PHOTORESIST
SiO_2
P- SUBSTRATE

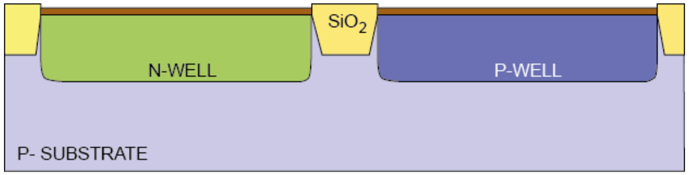
7. Ion implantation (Boron ~100 keV) -> P-well formation


PHOTORESIST
SiO$_2$
N-WELL
P- SUBSTRATE

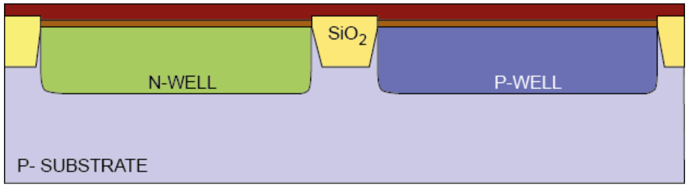
8. N-well and P-well are ready for implementing NMOS and PMOS transistors


SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

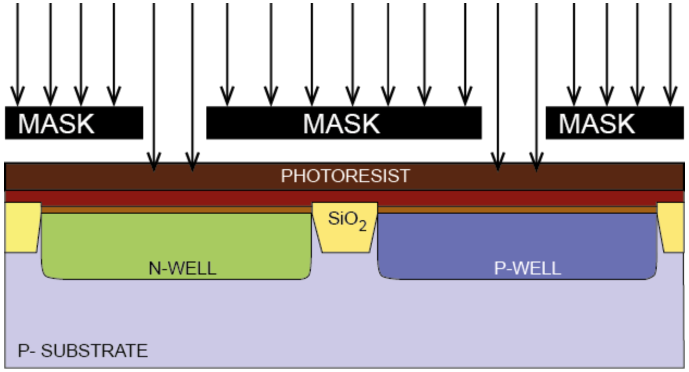
9. Gate oxide deposition


SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

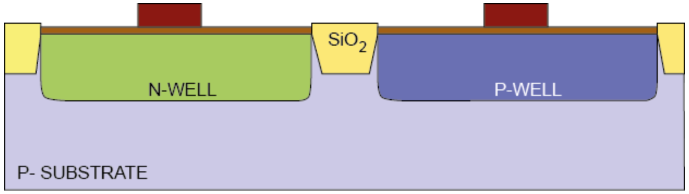
10. Deposition of polysilicon


SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

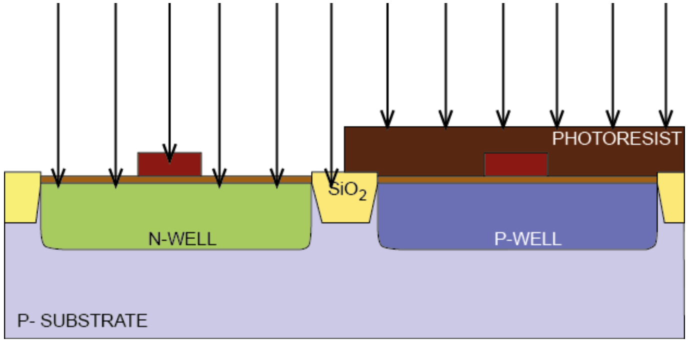
11. Photoresist deposition, illumination through mask


MASK
MASK
MASK
PHOTORESIST
SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

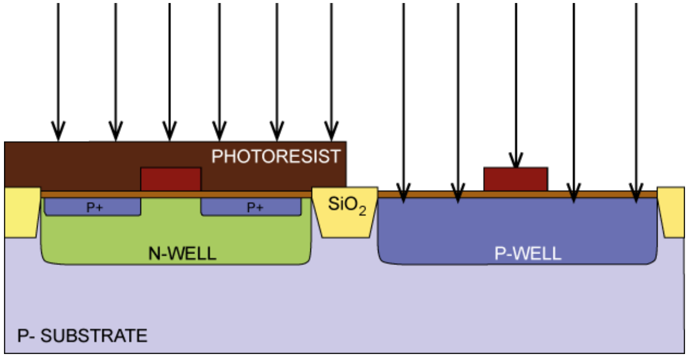
12. Gates are formed


SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

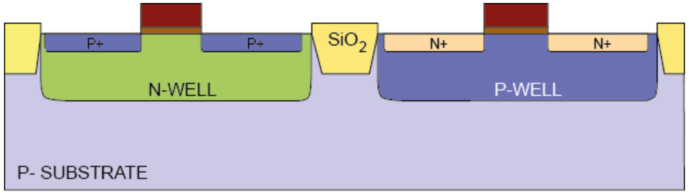
13. Low energy implantation of Boron dopants -> forming P+ regions of drain and source


PHOTORESIST
SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

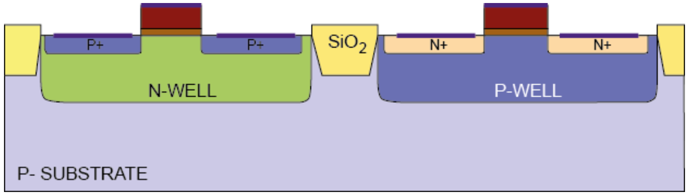
14. Low energy implantation of Phosphor dopants -> forming N+ regions of drain and source


PHOTORESIST
P+
P+
SiO$_2$
N-WELL
P-WELL
P- SUBSTRATE

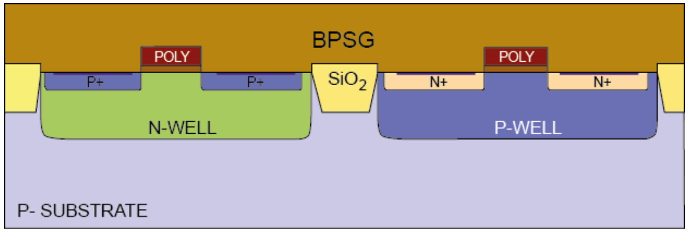
15. Removing photoresist and oxide from source and drain


P+
P+
SiO$_2$
N+
N+
N-WELL
P-WELL
P- SUBSTRATE

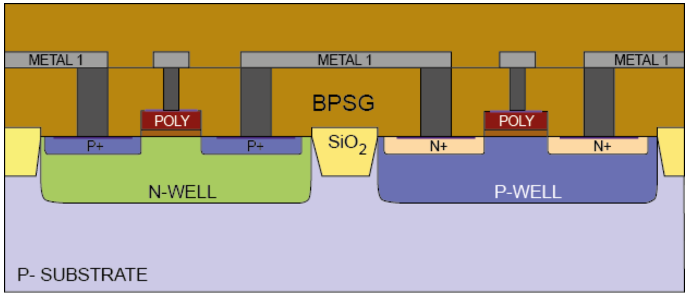
16. Silicidation


P+
P+
SiO$_2$
N+
N+
N-WELL
P-WELL
P- SUBSTRATE

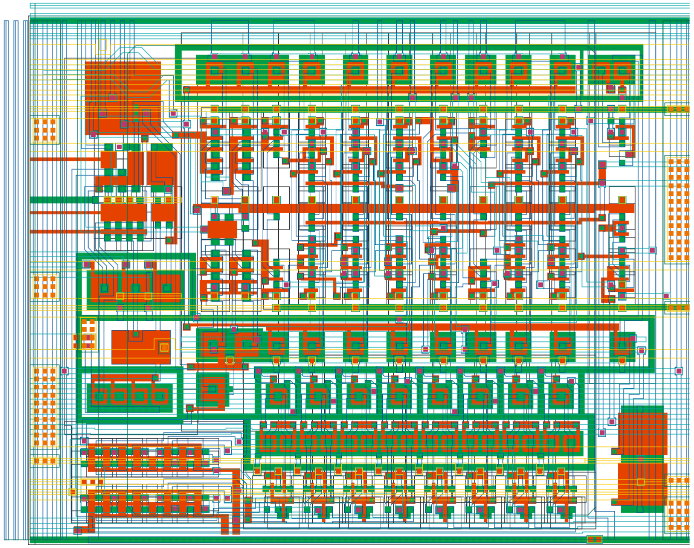
16. BPSG deposition


BPSG
POLY
POLY
P+
P+
SiO$_2$
N+
N+
N-WELL
P-WELL
P- SUBSTRATE

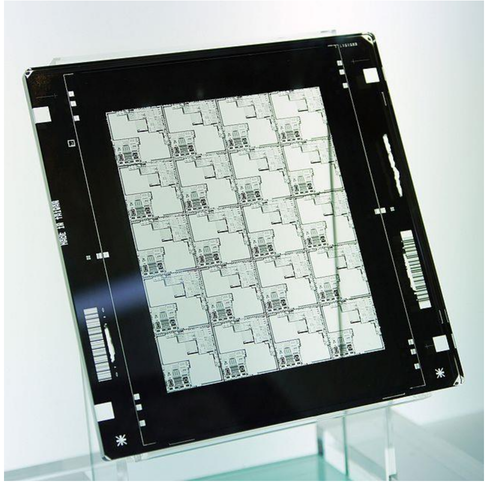
17. Etching, vias, deposition of METAL1, BPSG isolation


METAL 1
METAL 1
METAL 1
BPSG
POLY
POLY
P+
P+
SiO$_2$
N+
N+
N-WELL
P-WELL
P- SUBSTRATE

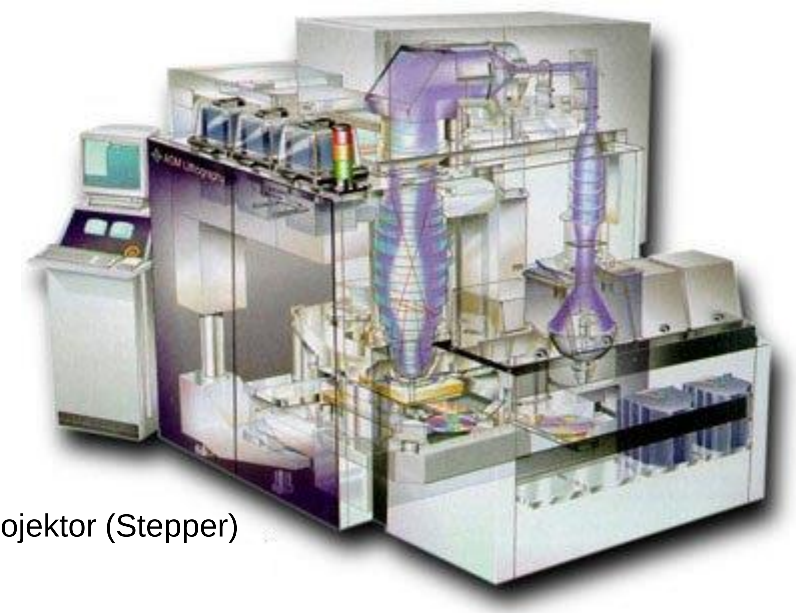
- Layout -> Fotomaske -> IC



Layout

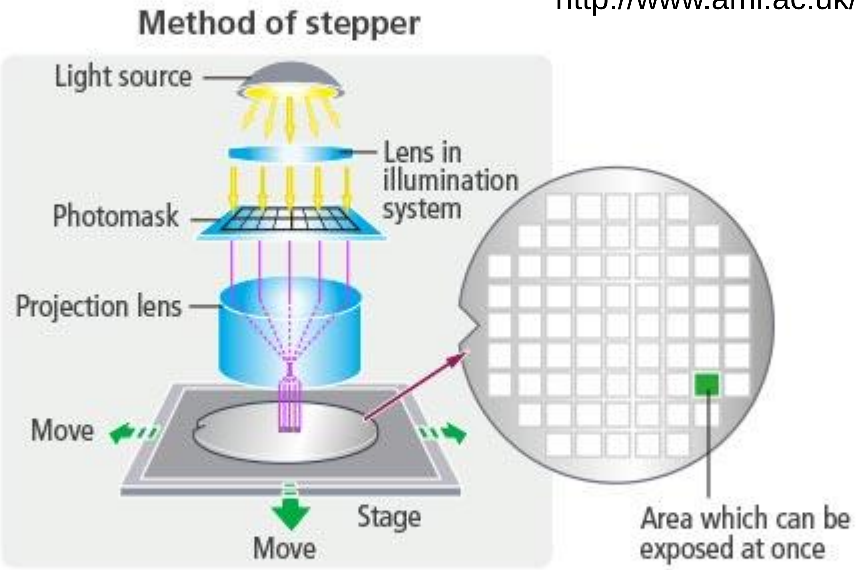


Maske

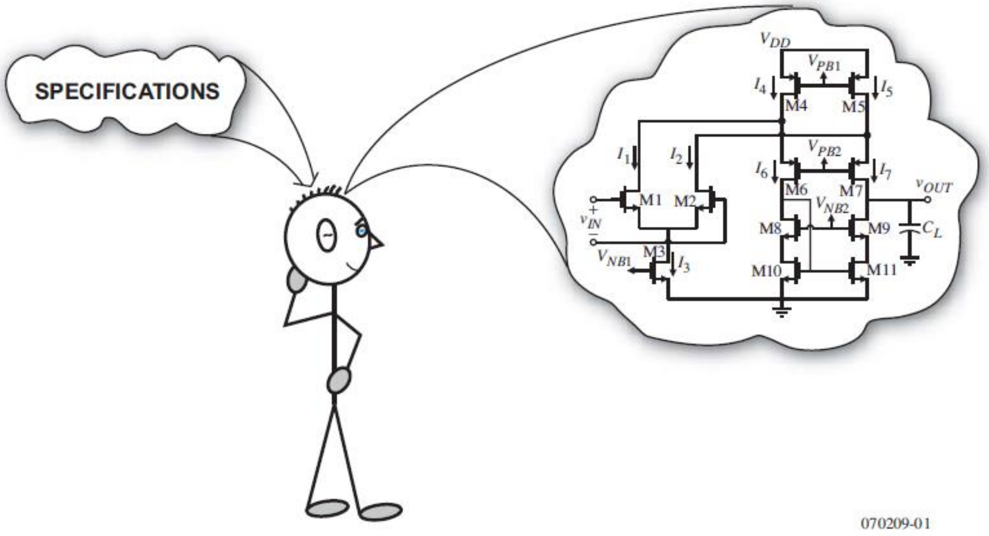


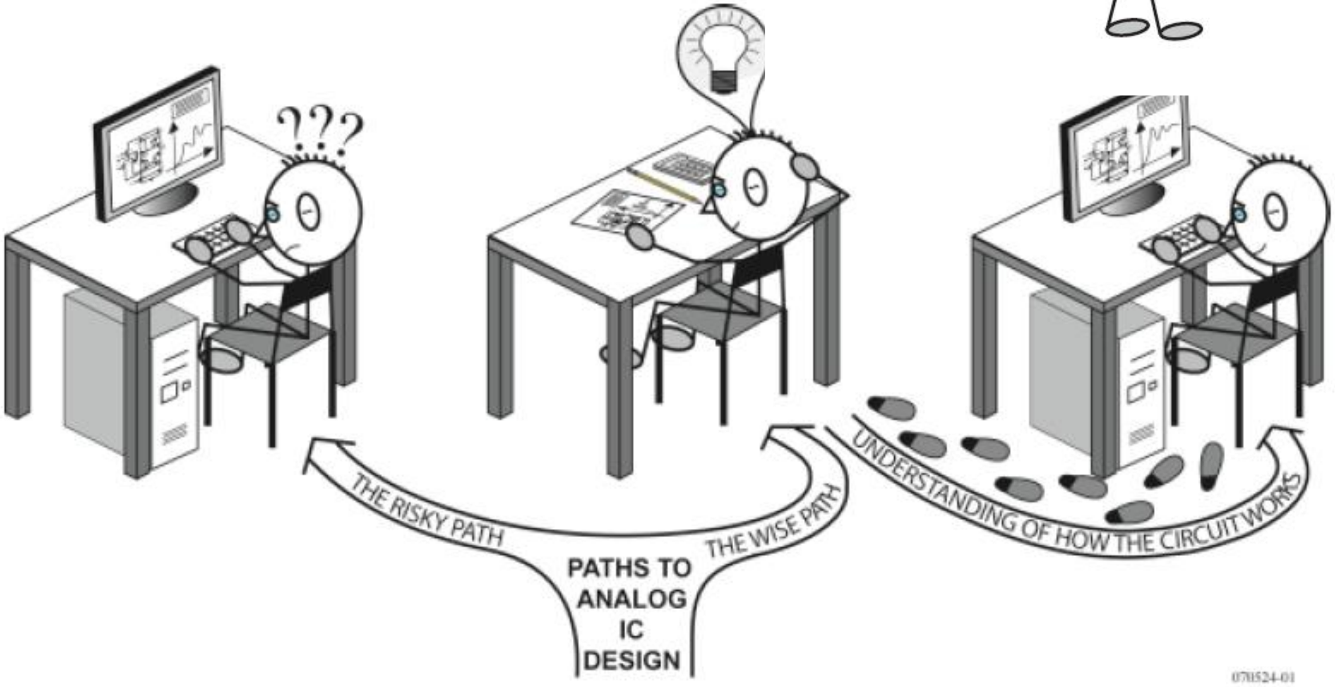
Projektor (Stepper)

http://www.ami.ac.uk/courses/


Method of stepper
Light source
Lens in illumination system
Photomask
Projection lens
Move
Move
Stage
Move
Area which can be exposed at once

- IC Design Software (z.B. Cadence)
- Analog- und Digital-Design-Flow
- Spezifikationen
- Systemkonzept
- Schaltungstechnische Realisierung
- Wichtig (P.E. Allen):
- zuerst Schaltung verstehen
- und danach sich vorm PC setzten


SPECIFICATIONS
V_{DD}
V_{PB1}
I_4
I_5
M4
M5
V_{PB2}
I_1
I_2
I_6
I_7
M1
M2
M6
M7
v_{OUT}
V_{NB2}
v_{IN}
M8
M9
C_L
V_{NB1}
M3
I_3
M10
M11
070209-01


???
THE RISKY PATH
THE WISE PATH
UNDERSTANDING OF HOW THE CIRCUIT WORKS
PATHS TO ANALOG IC DESIGN
070524-01

- Chiphersteller wählen („foundry“)

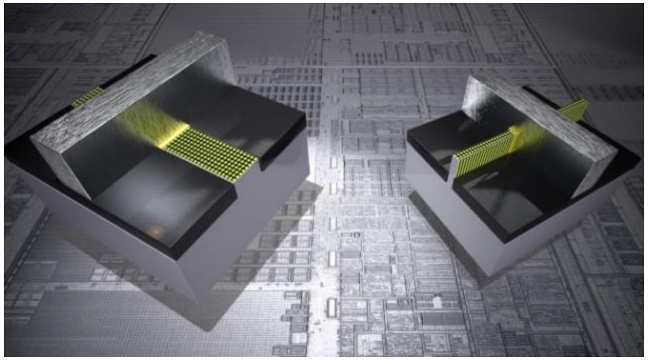
AMS

TSMC

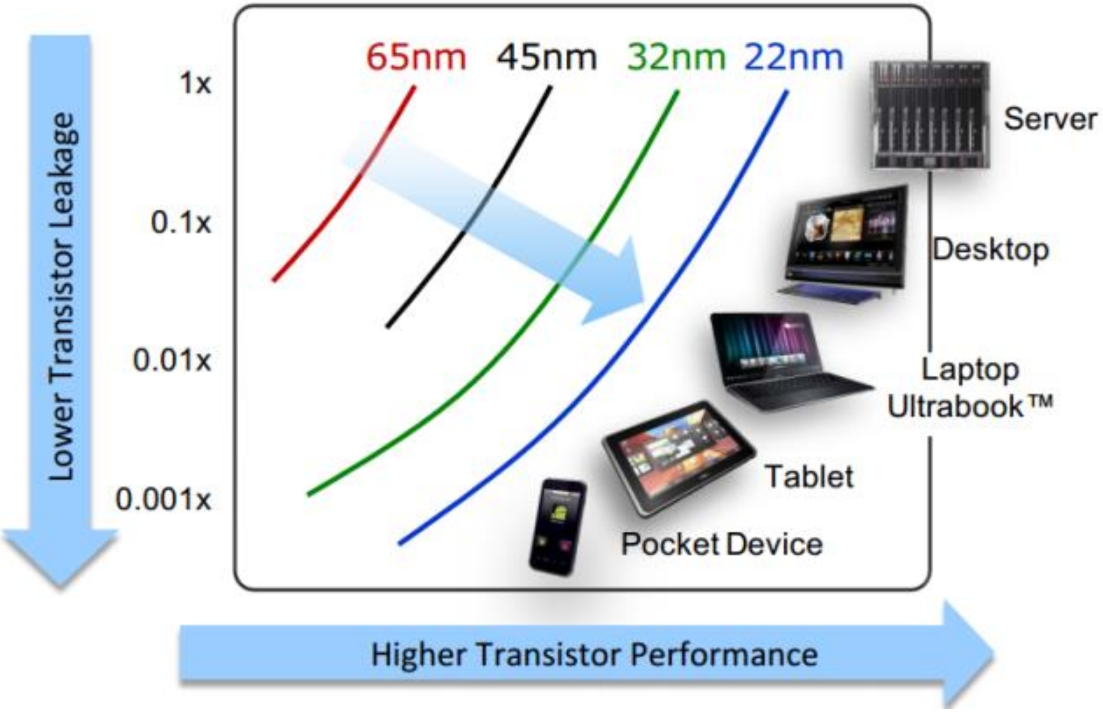
X-FAB Dresden

UMC

- Prozess wählen
- CMOS (digital, opto, analog, RF)
- Prozesse:
- SOI, BiCMOS, HVCMOS, FINFET, FD SOI
- Process nodes:
- 0.35 um, 0.18um, 0.13um, 90nm, 65nm, 40nm, 28nm…
- Kleinere Prozesse – analog Design schwieriger
- Europractice: Multi Project Runs

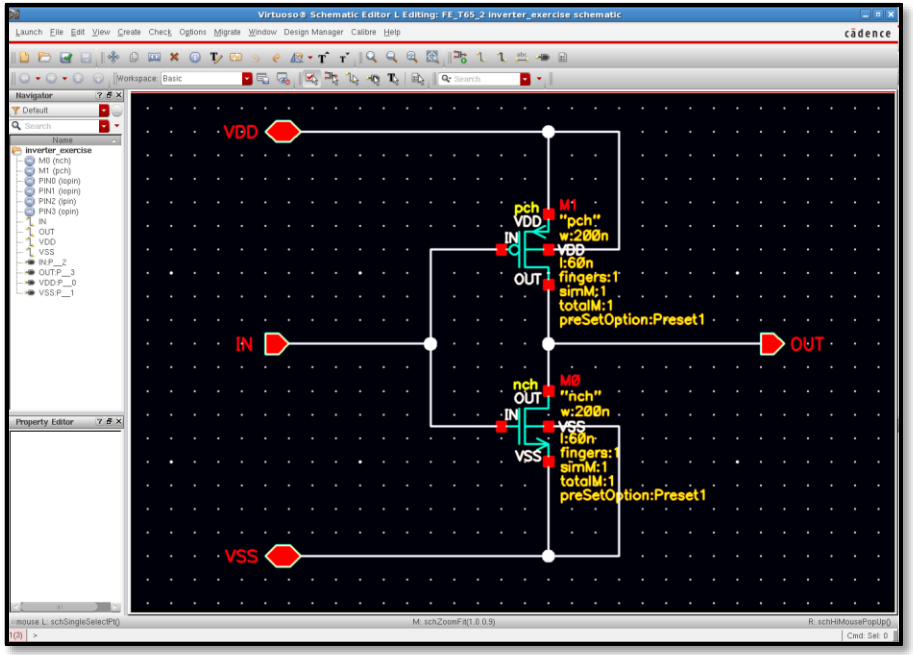


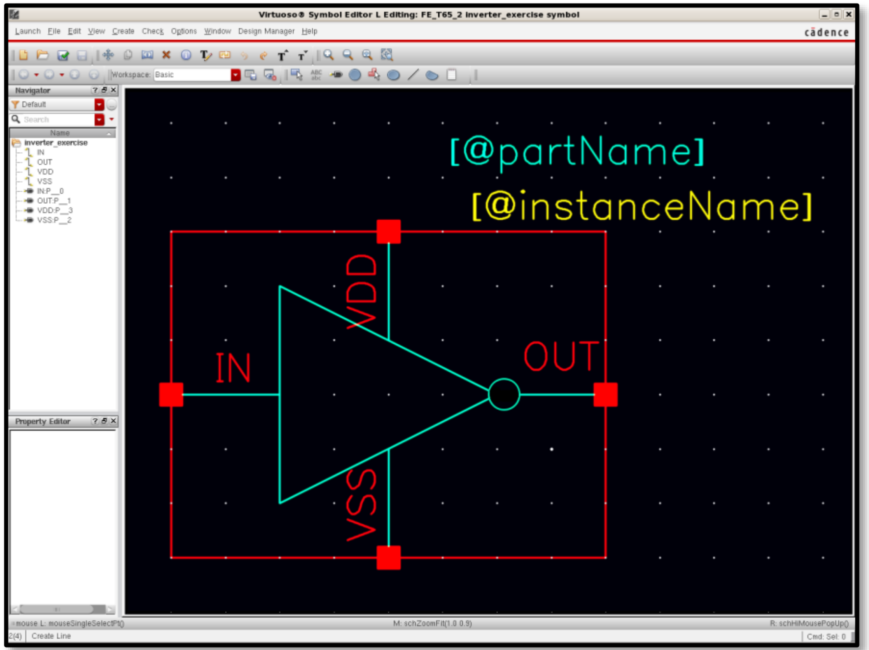
http://www.extremetech.com/



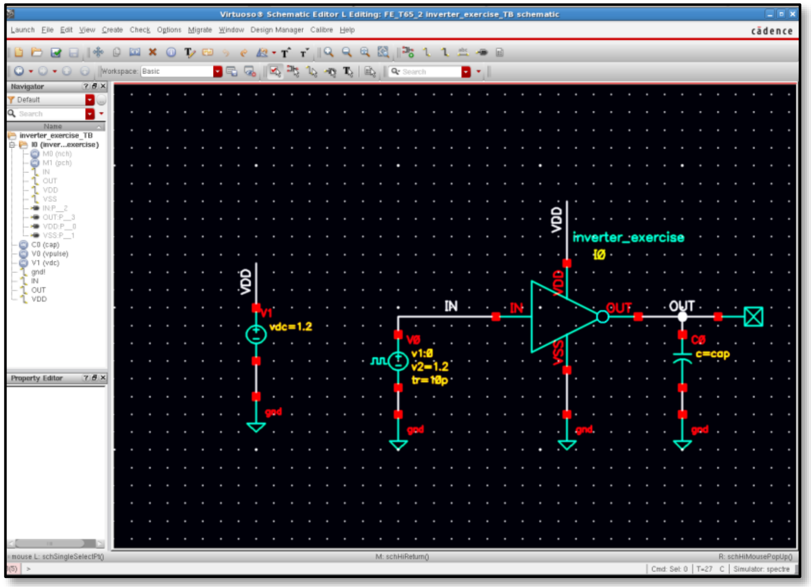
- Simulationsmodelle
- Layout-Regeln
- Process Design Kit (PDK) – Prozess-Bibliothek
- http://www.europractice-ic.com/

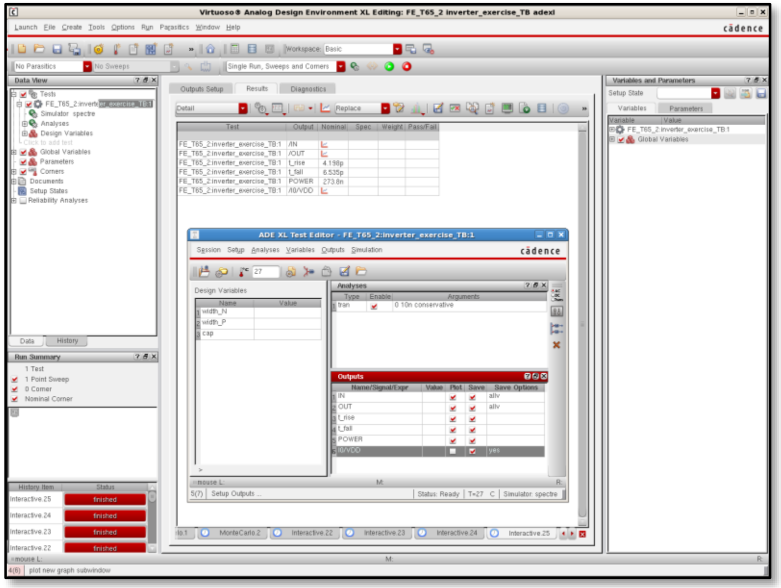
- Schaltplanentwurf im Schematics Editor
- Transistor, Hierarchie, Inputs/Outputs
- Symbol wird generiert – hierarchische Designs

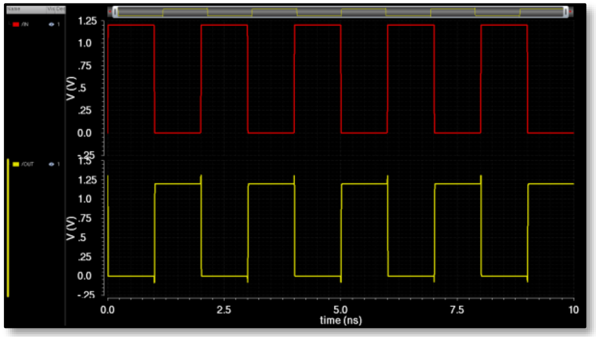

Virtuoso® Schematic Editor L Editing: FE_T65_2 inverter_exercise schematic
Launch File Edit View Create Check Options Migrate Window Design Manager Calibre Help
cādence
Workspace: Basic
Search
Navigator
Default
Search
Name
inverter_exercise
M0 (nch)
M1 (pch)
PIN0 (iopin)
PIN1 (iopin)
PIN2 (ipin)
PIN3 (opin)
IN
OUT
VDD
VSS
IN:P__2
OUT:P__3
VDD:P__0
VSS:P__1
Property Editor
VDD
pch
VDD
IN
OUT
M1
"pch"
w:200n
VDD
l:60n
fingers:1
simM:1
totalM:1
preSetOption:Preset1
IN
OUT
nch
OUT
IN
VSS
M0
"nch"
w:200n
VSS
l:60n
fingers:1
simM:1
totalM:1
preSetOption:Preset1
VSS
mouse L: schSingleSelectPt()
M: schZoomFit(1.0 0.9)
R: schHiMousePopUp()
1(3) >
Cmd: Sel: 0


Virtuoso® Symbol Editor L Editing: FE_T65_2 inverter_exercise symbol
Launch File Edit View Create Check Options Window Design Manager Help
cādence
Workspace: Basic
Navigator
Default
Search
Name
inverter_exercise
IN
OUT
VDD
VSS
IN:P__0
OUT:P__1
VDD:P__3
VSS:P__2
Property Editor
[@partName]
[@instanceName]
VDD
IN
OUT
VSS
mouse L: mouseSingleSelectPt()
M: schZoomFit(1.0 0.9)
R: schHiMousePopUp()
2(4) Create Line
Cmd: Sel: 0

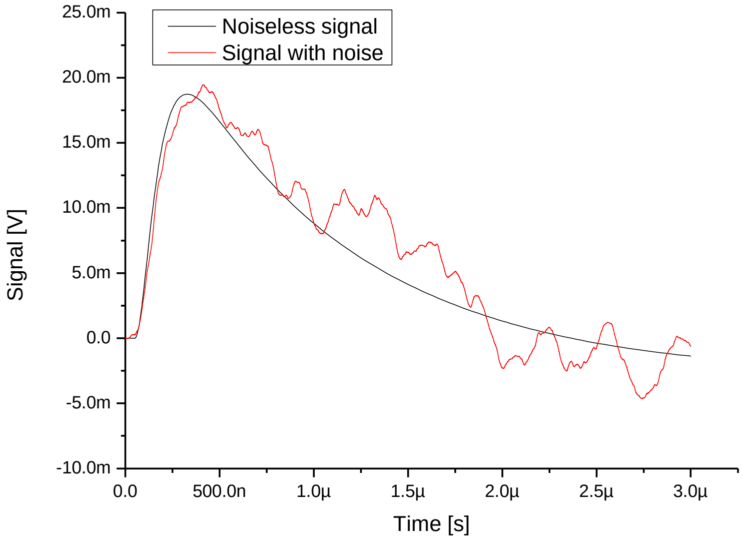
- Schaltung wird simuliert
- Analoge, mixed-mode- oder digitale Simulation
- AC, DC, Großsignale (Transient Analysis)

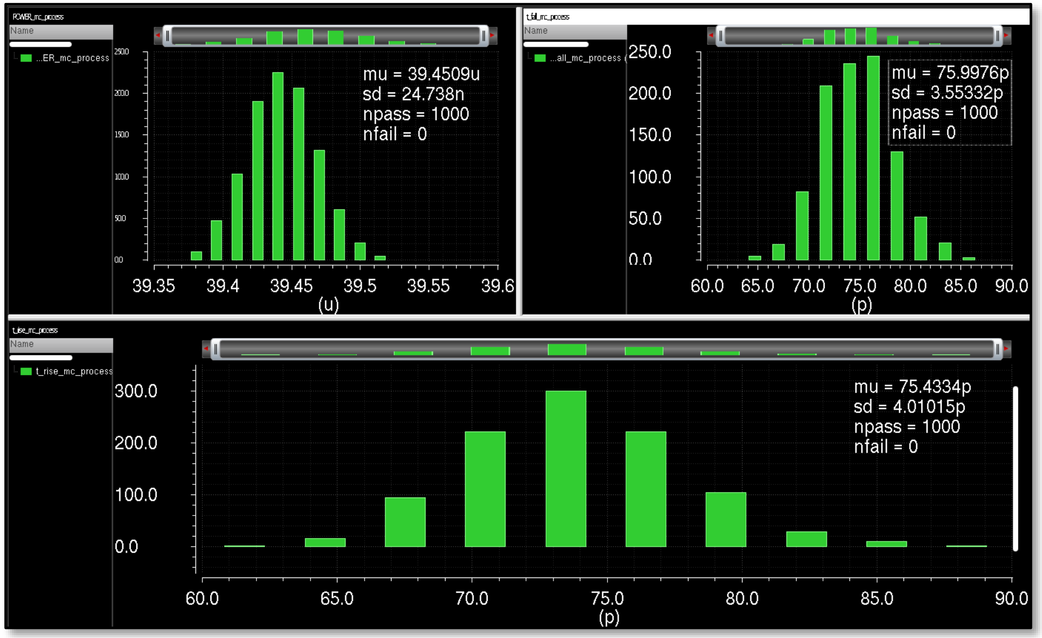

Virtuoso® Schematic Editor L Editing: FE_T65_2 inverter_exercise_TB schematic
Launch File Edit View Create Check Options Migrate Window Design Manager Calibre Help
cadence
Navigator
Property Editor
VDD
V1
vdc=1.2
gnd
IN
V0
v1:0
v2=1.2
tr=10p
inverter_exercise
I0
VDD
VSS
OUT
C0
c=cap


Virtuoso® Analog Design Environment XL Editing: FE_T65_2 inverter_exercise_TB adexl
Launch File Create Tools Options Run Parasitics Window Help
cadence
Data View
Outputs Setup
Results
Diagnostics
Variables and Parameters
ADE XL Test Editor - FE_T65_2:inverter_exercise_TB:1
Session Setup Analyses Variables Outputs Simulation
Design Variables
Analyses
Outputs
Run Summary



- Rauschen
- Mismatch



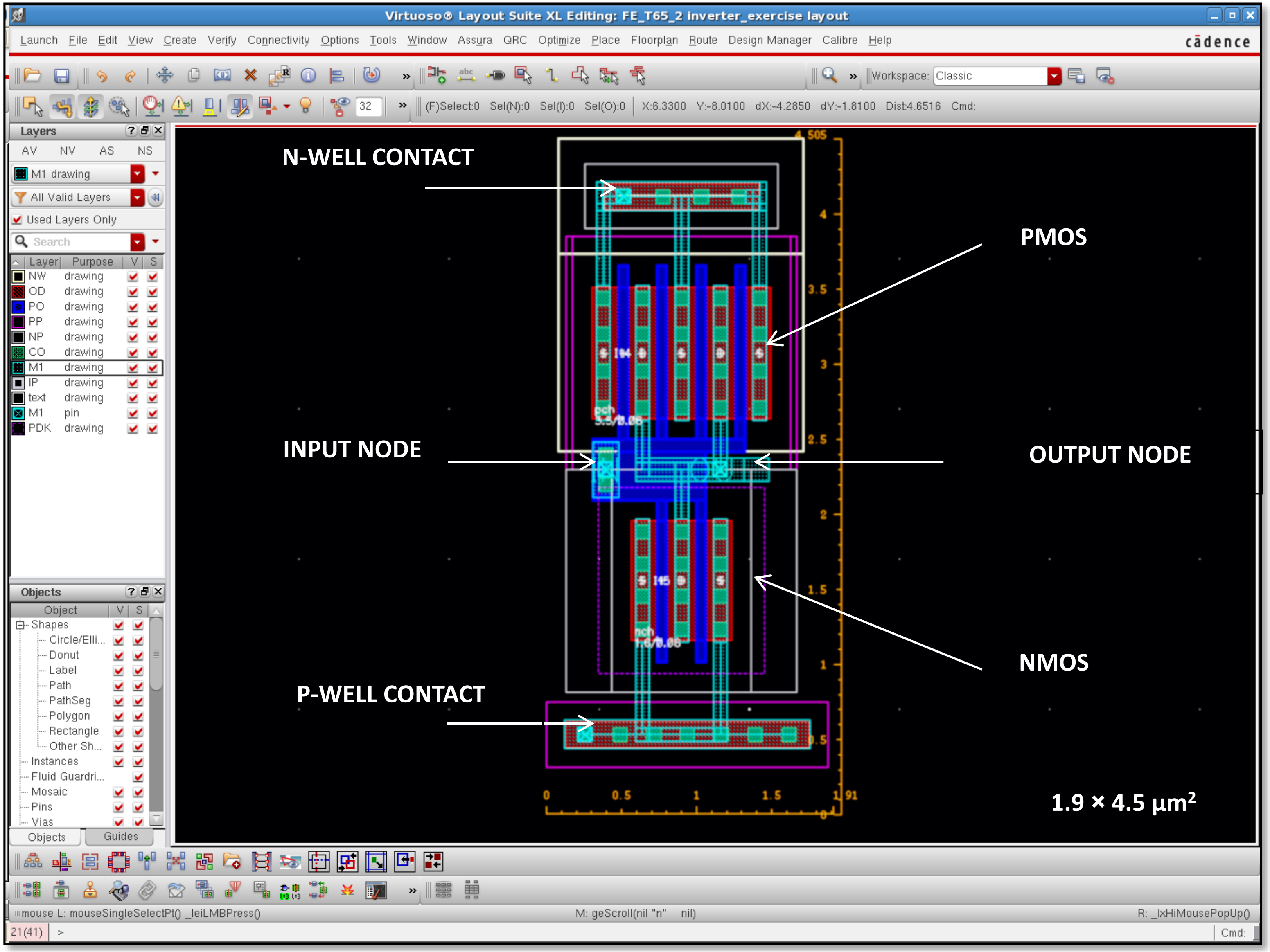

Name
...ER_mc_process
2500
2000
1500
1000
500
0.0
39.35
39.4
39.45
39.5
39.55
39.6
(u)
Name
...all_mc_process
250.0
200.0
150.0
100.0
50.0
0.0
60.0
65.0
70.0
75.0
80.0
85.0
90.0
(p)
Name
t_rise_mc_process
300.0
200.0
100.0
0.0
60.0
65.0
70.0
75.0
80.0
85.0
90.0
(p)

```
mu = 39.4509u
sd = 24.738n
npass = 1000
nfail = 0
```

```
mu = 75.9976p
sd = 3.55332p
npass = 1000
nfail = 0
```

```
mu = 75.4334p
sd = 4.01015p
npass = 1000
nfail = 0
```

- Layout-Design
- Masken
- Transistoren „von oben“
- Analog Design – Full-Custom Layout (Hand-Layouted)


Launch File Edit View Create Verify Connectivity Options Tools Window Assura QRC Optimize Place Floorplan Route Design Manager Calibre Help
cādence
Layers
AV NV AS NS
M1 drawing
All Valid Layers
Search
Objects
Guides
4.505
4
3.5
3
2.5
2
1.5
1
0.5
0
0
0.5
1
1.5
1.91
I14
pch
3.5/0.06
I15
nch
1.6/0.06

Virtuoso® Layout Suite XL Editing: FE_T65_2 inverter_exercise layout

Workspace: Classic

(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:6.3300 Y:-8.0100 dX:-4.2850 dY:-1.8100 Dist:4.6516 Cmd:

☑ Used Layers Only

Layer	Purpose	V	S
NW	drawing	☑	☑
OD	drawing	☑	☑
PO	drawing	☑	☑
PP	drawing	☑	☑
NP	drawing	☑	☑
CO	drawing	☑	☑
M1	drawing	☑	☑
IP	drawing	☑	☑
text	drawing	☑	☑
M1	pin	☑	☑
PDK	drawing	☑	☑

Object	V	S
Shapes	☑	☑
Circle/Elli...	☑	☑
Donut	☑	☑
Label	☑	☑
Path	☑	☑
PathSeg	☑	☑
Polygon	☑	☑
Rectangle	☑	☑
Other Sh...	☑	☑
Instances	☑	☑
Fluid Guardri...		☑
Mosaic	☑	☑
Pins	☑	☑
Vias	☑	☑

mouse L: mouseSingleSelectPt() _leiLMBPress() M: geScroll(nil "n" nil) R: _lxHiMousePopUp()

21(41) >

Cmd:

N-WELL CONTACT

PMOS

INPUT NODE

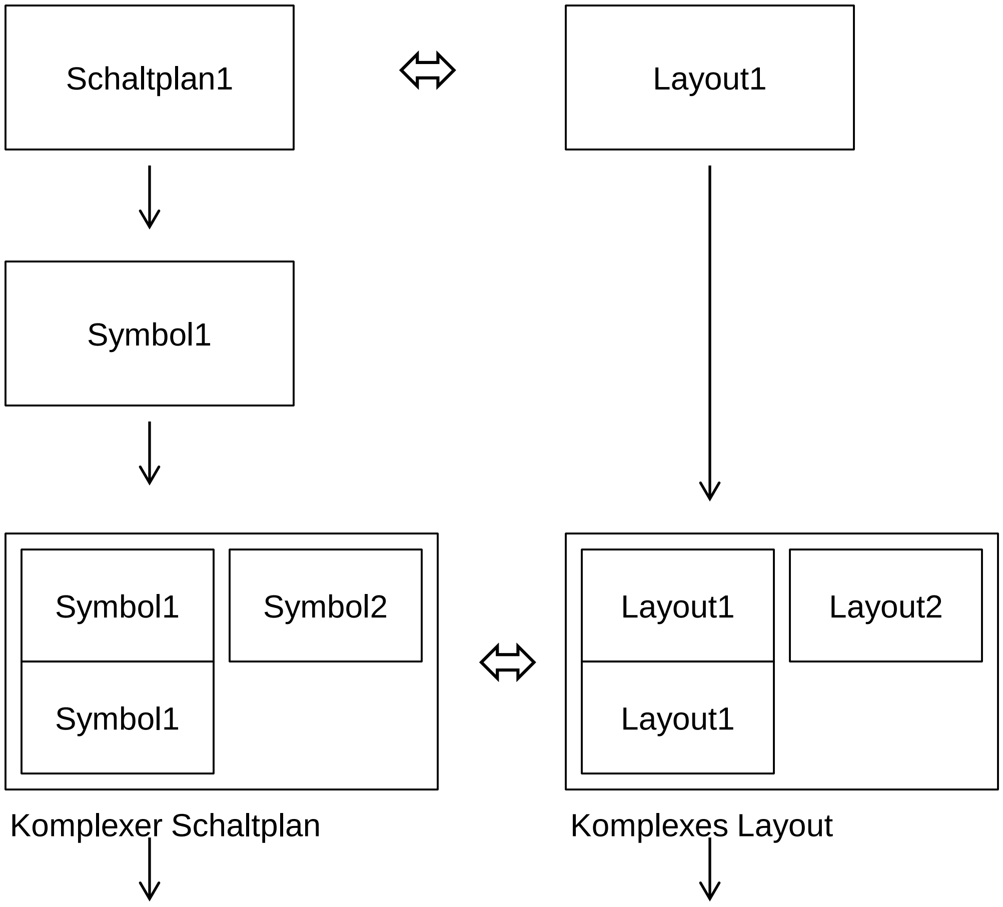
OUTPUT NODE

NMOS

P-WELL CONTACT

1.9 × 4.5 µm²

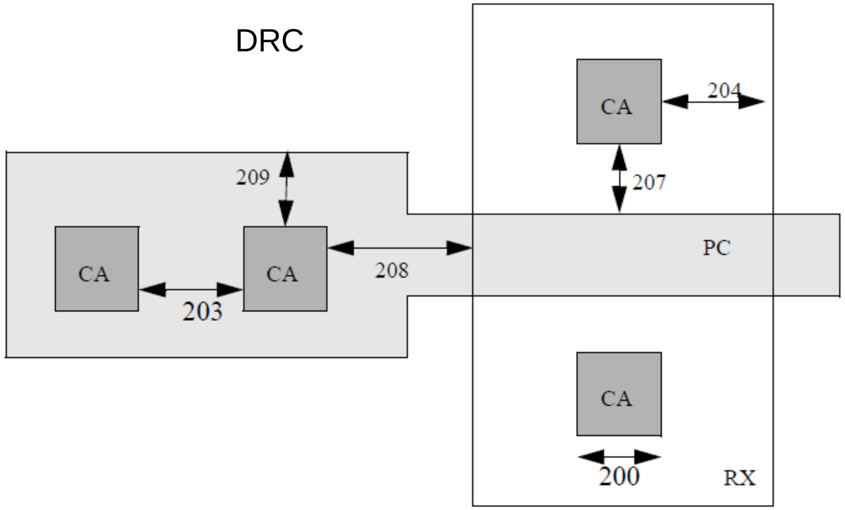
- Layout-Editor
- Polygone, Pfade
- Zellen, Blöcke, Hierarchie
- Semiautomatische Generierung von Layouts aus dem Schaltplan ist möglich



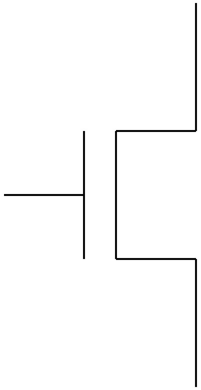
Schaltplan1
⇔
Layout1
Symbol1
Symbol1
Symbol2
Symbol1
⇔
Layout1
Layout2
Layout1
Komplexer Schaltplan
Komplexes Layout

- Layout-Regeln (Teil vom PDK)
- DRC Überprüfung von Layout-Regeln
- LVS Layout Schaltplan Vergleich
- Layout -> Netzliste <-> Netzliste <- Schaltplan
- Extraktion von Kapazitäten aus Layout
- Post-Layout Simulation
- Evt. Anpassung vom Schaltplan notwendig

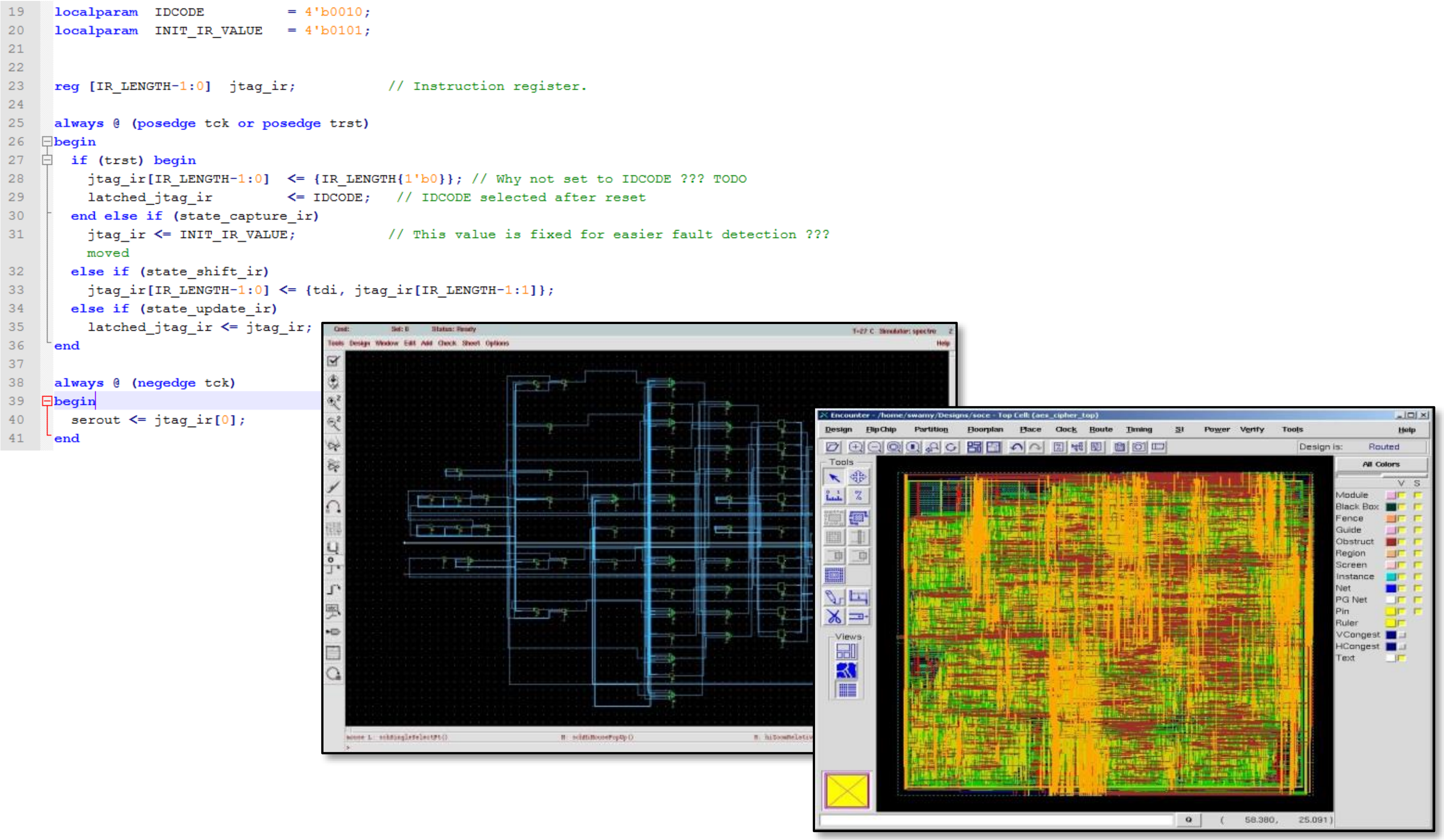
DRC


CA
204
209
207
CA
CA
208
PC
203
CA
200
RX

LVS



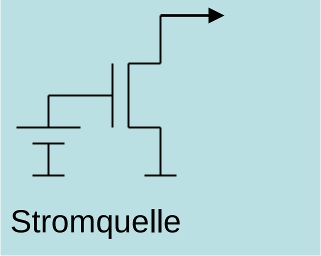
- Digitaldesign
- HDL Code, Simulation -> RTL Code (Schaltplan mit Logikzellen und Registern), Simulation (automatisch) -> Layout, Simulation (automatisch) -> DRC, LVS

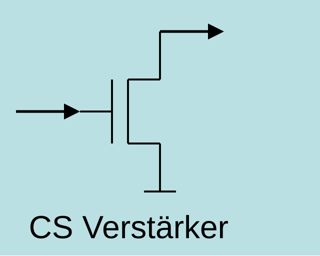


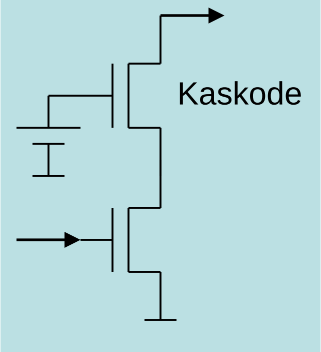
```
localparam  IDCODE          = 4'b0010;
localparam  INIT_IR_VALUE   = 4'b0101;


reg [IR_LENGTH-1:0]  jtag_ir;           // Instruction register.

always @ (posedge tck or posedge trst)
begin
  if (trst) begin
    jtag_ir[IR_LENGTH-1:0]  <= {IR_LENGTH{1'b0}}; // Why not set to IDCODE ??? TODO
    latched_jtag_ir         <= IDCODE;   // IDCODE selected after reset
  end else if (state_capture_ir)
    jtag_ir <= INIT_IR_VALUE;           // This value is fixed for easier fault detection ???
    moved
  else if (state_shift_ir)
    jtag_ir[IR_LENGTH-1:0] <= {tdi, jtag_ir[IR_LENGTH-1:1]};
  else if (state_update_ir)
    latched_jtag_ir <= jtag_ir;
end

always @ (negedge tck)
begin
  serout <= jtag_ir[0];
end
```

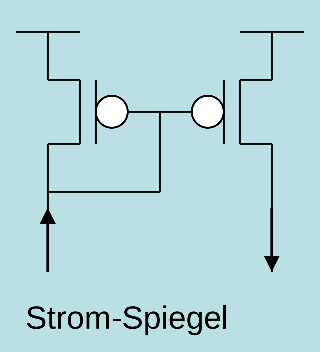
Cmd:
Sel: 0
Status: Ready
T=27 C
Simulator: spectre
Tools Design Window Edit Add Check Sheet Options
Help
Encounter - /home/swamy/Designs/soce - Top Cell: (aes_cipher_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools
Help
Design is: Routed
All Colors
Tools
Views
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
PG Net
Pin
Ruler
VCongest
HCongest
Text
58.380, 25.091

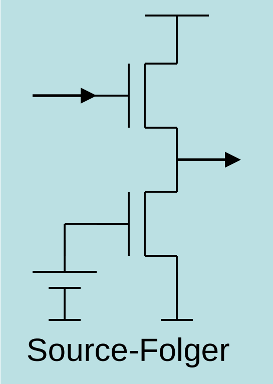
- Schaltungsentwurf
- Tricks:
- Gute Strukturierung
- Verwendung von Grundschaltungen
- Bausteinprinzip

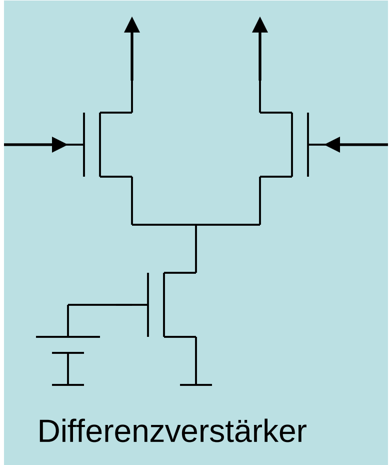

Stromquelle


CS Verstärker

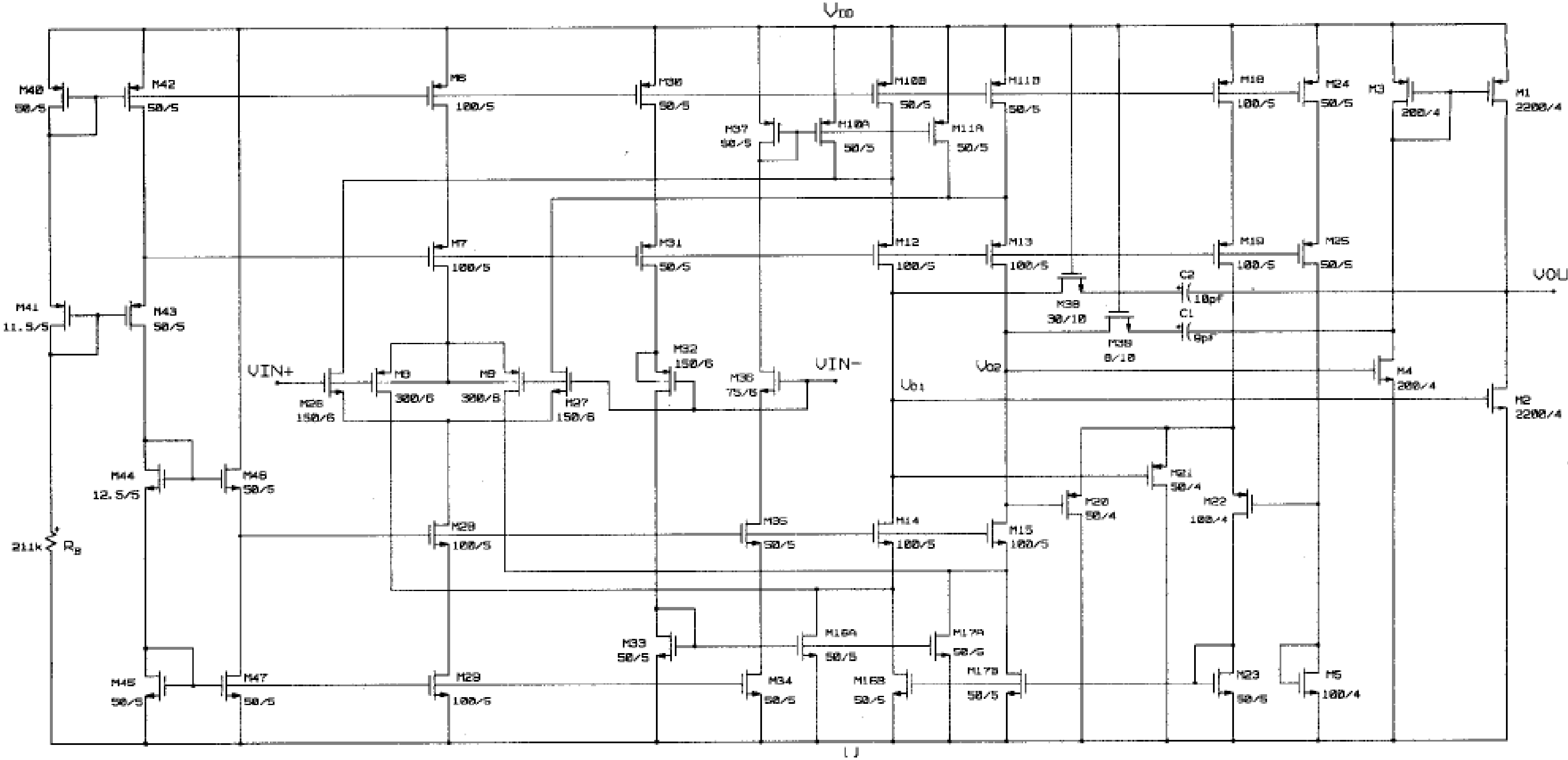

Kaskode


Strom-Spiegel


Source-Folger


Differenzverstärker

- Verwendung von Grundschaltungen

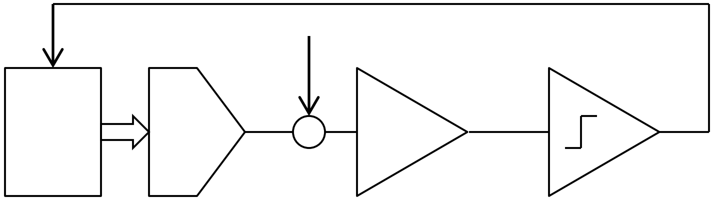

VDD
M40
50/5
M42
50/5
M6
100/5
M30
50/5
M37
50/5
M10A
50/5
M10B
50/5
M11A
50/5
M11B
50/5
M18
100/5
M24
50/5
M3
200/4
M1
2200/4
M7
100/5
M31
50/5
M12
100/5
M13
100/5
M19
100/5
M25
50/5
VOUT
C2
10pF
M38
30/10
C1
8pF
M39
8/10
M41
11.5/5
M43
50/5
VIN+
M26
150/6
M8
300/6
M9
300/6
M27
150/6
M32
150/6
M36
75/6
VIN-
Vb2
Vb1
M4
200/4
M2
2200/4
M44
12.5/5
M46
50/5
M21
50/4
M20
50/4
M22
100/4
211k
RB
M28
100/5
M35
50/5
M14
100/5
M15
100/5
M33
50/5
M16A
50/5
M17A
50/5
M45
50/5
M47
50/5
M29
100/5
M34
50/5
M16B
50/5
M17B
50/5
M23
50/5
M5
100/4

Rail to rail CMOS Opamp: IEEE Journal of Solid-State Circuits, vol. 23, pp. 1414 – 1417, December 1988

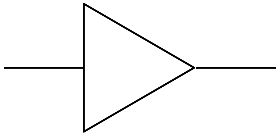
- Hierarchie im Chip

Chip (Integrierte Schaltung)

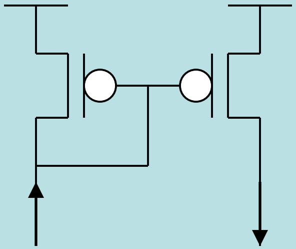
Systeme



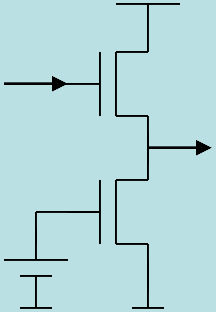
Schaltungen



Grundschaltungen

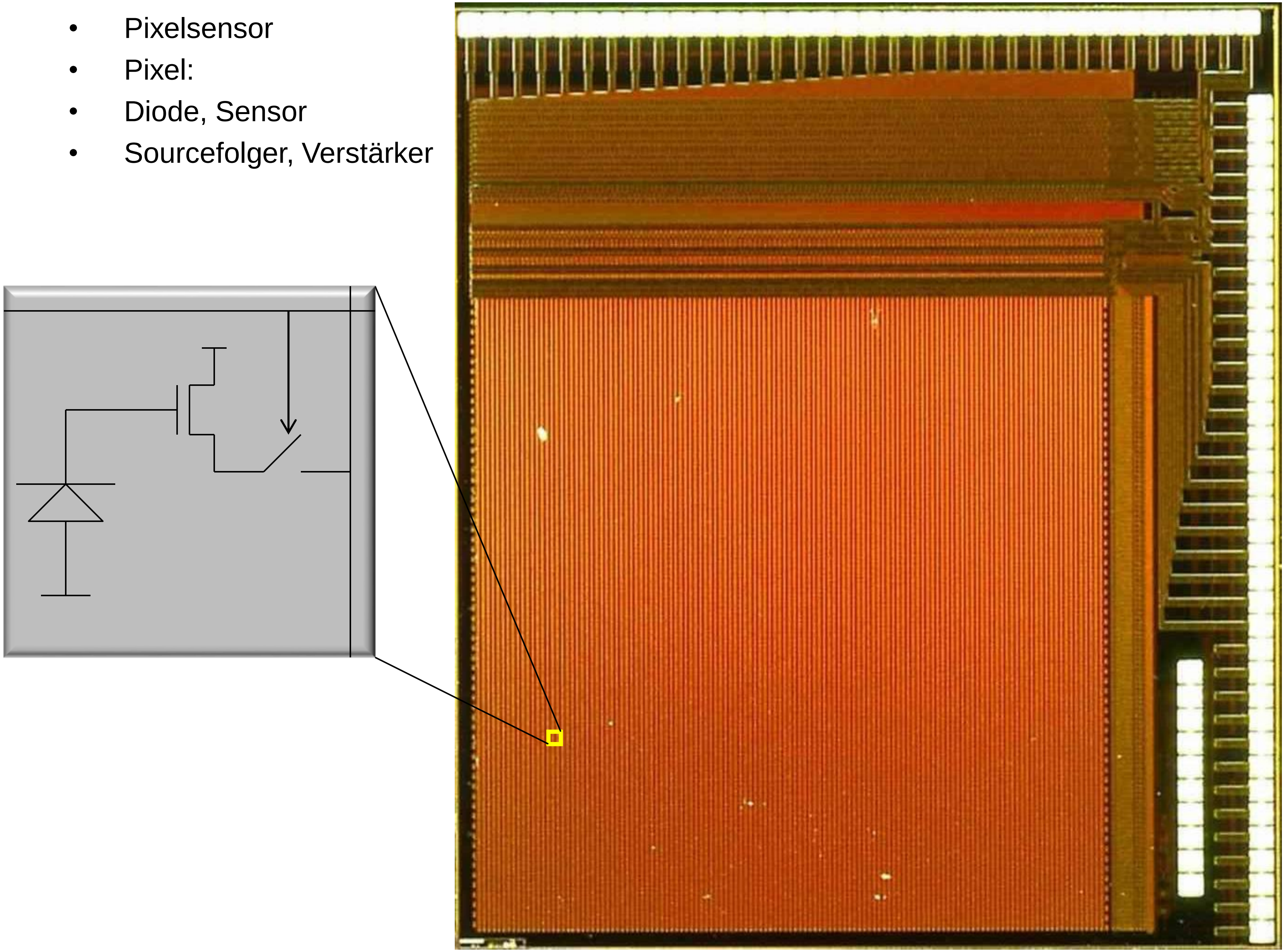


Strom-Spiegel

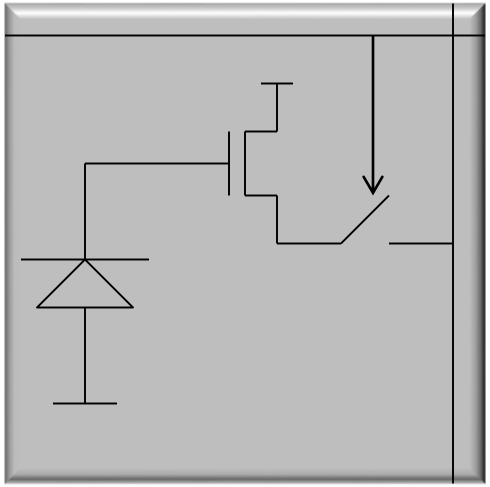


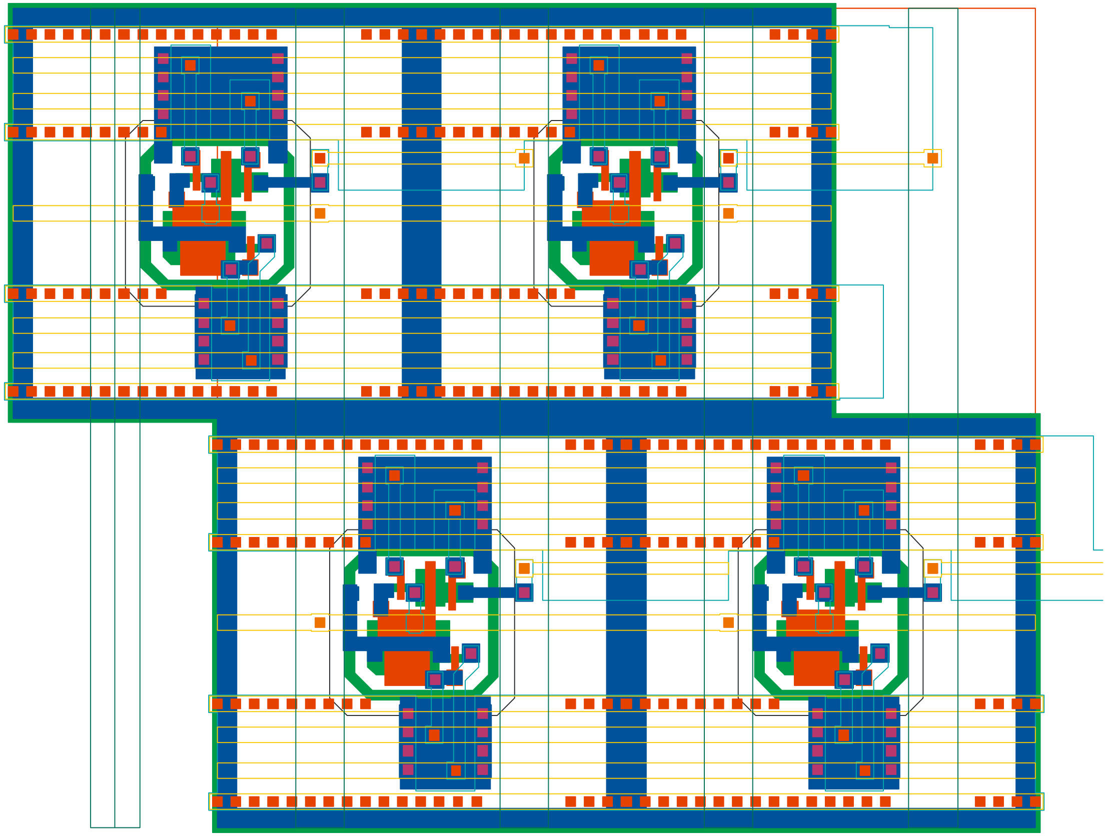
Source-Folger

- Pixelsensor
- Pixel:
- Diode, Sensor
- Sourcefolger, Verstärker

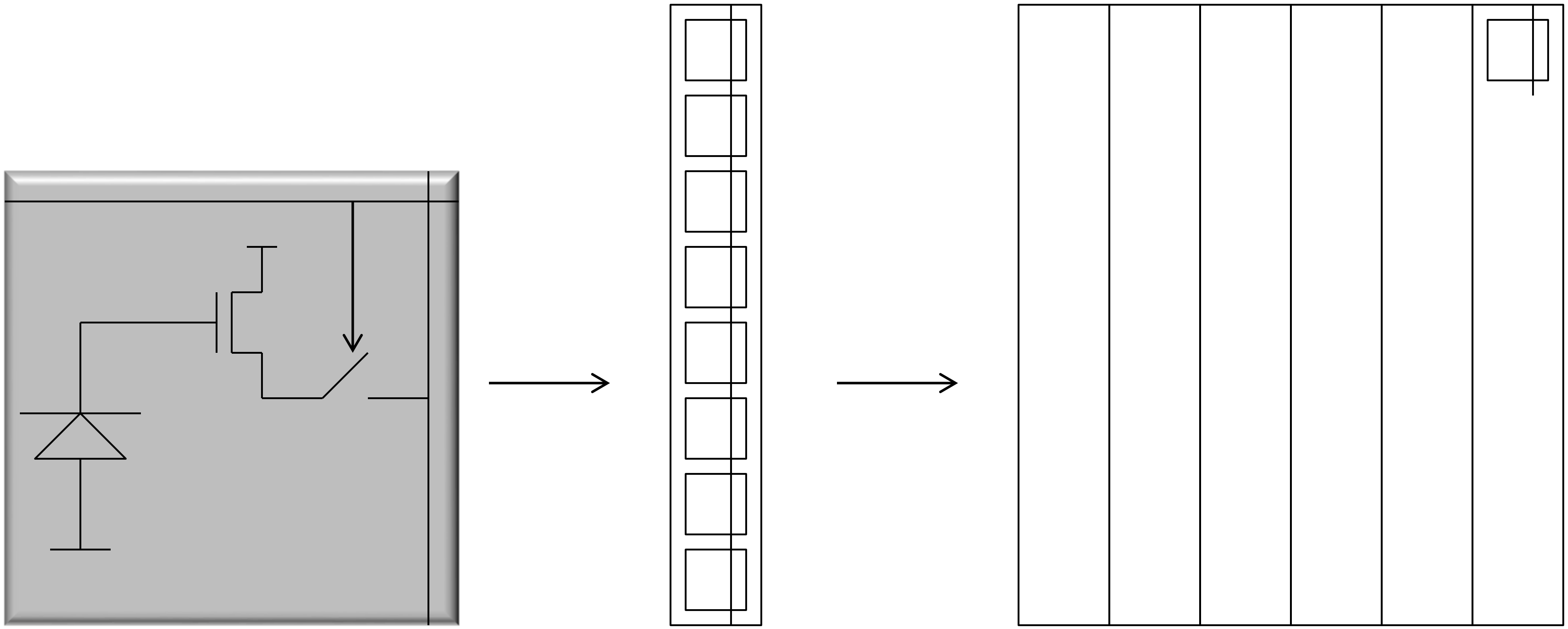


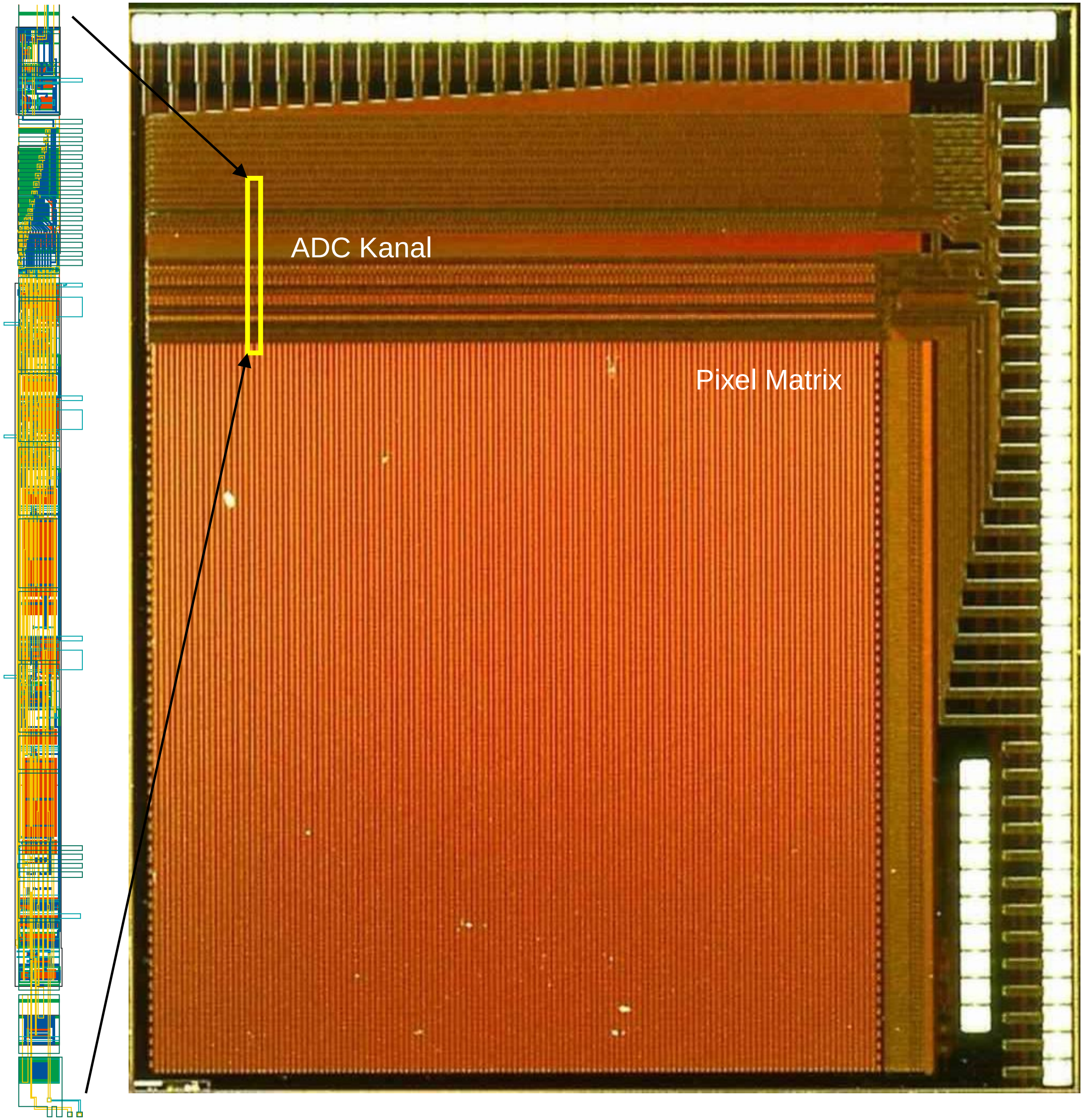
- Pixel Schaltplan
- Pixel Layout
- DRC, LVS



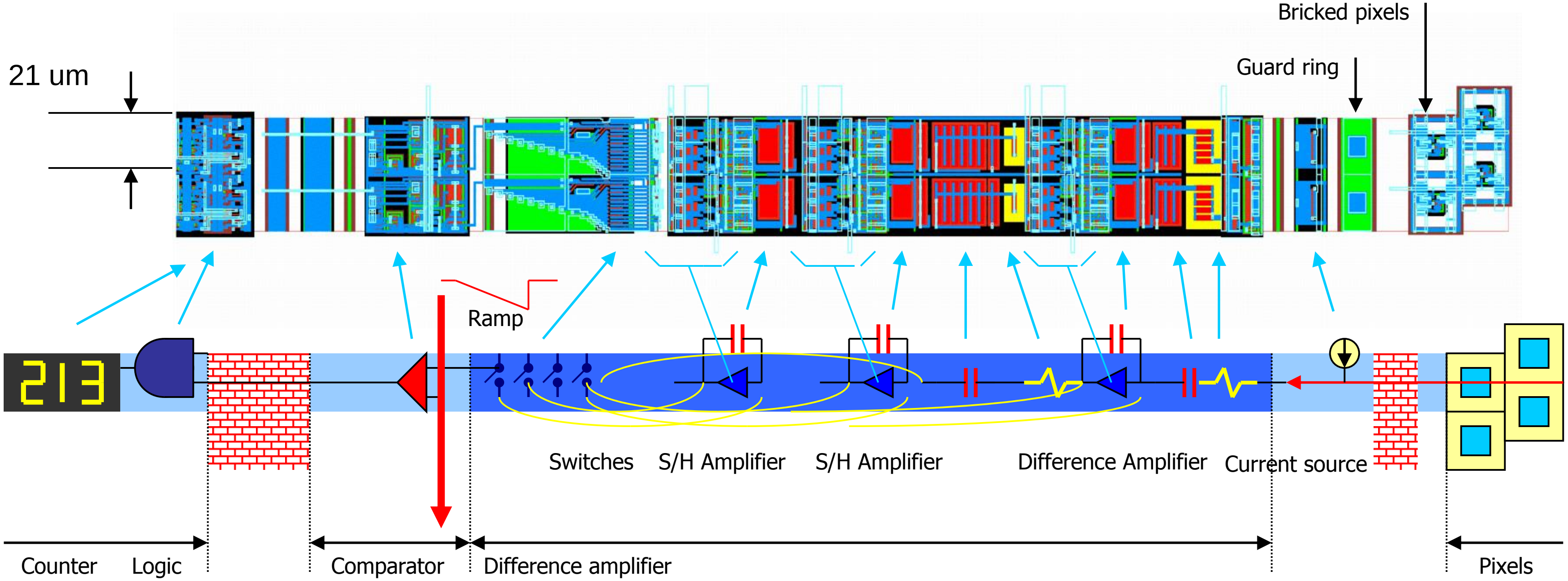


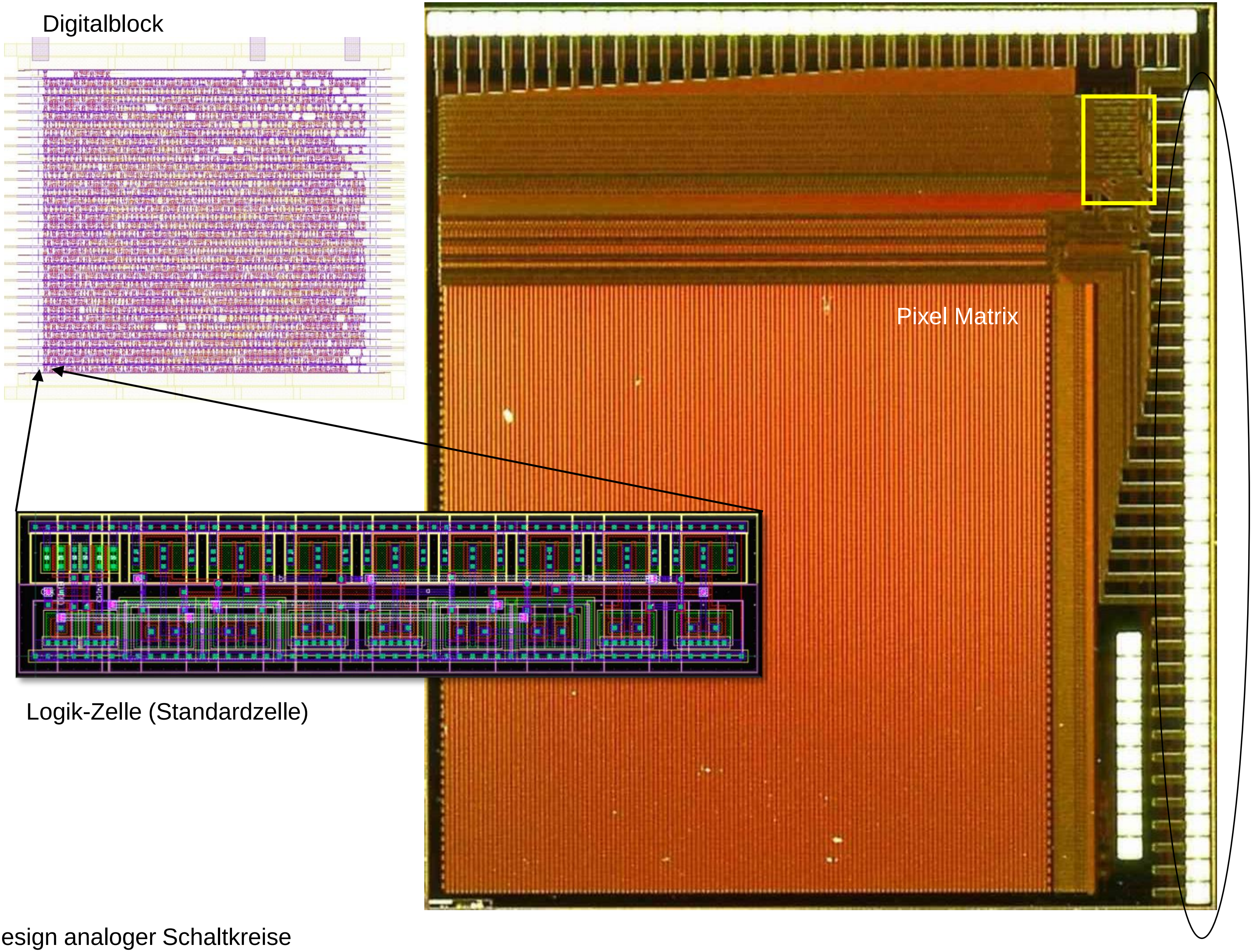
- Pixel
- Pixel Spalte
- Pixel Matrix



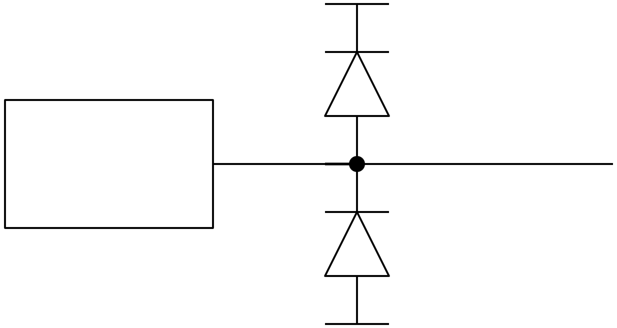

ADC Kanal
Pixel Matrix

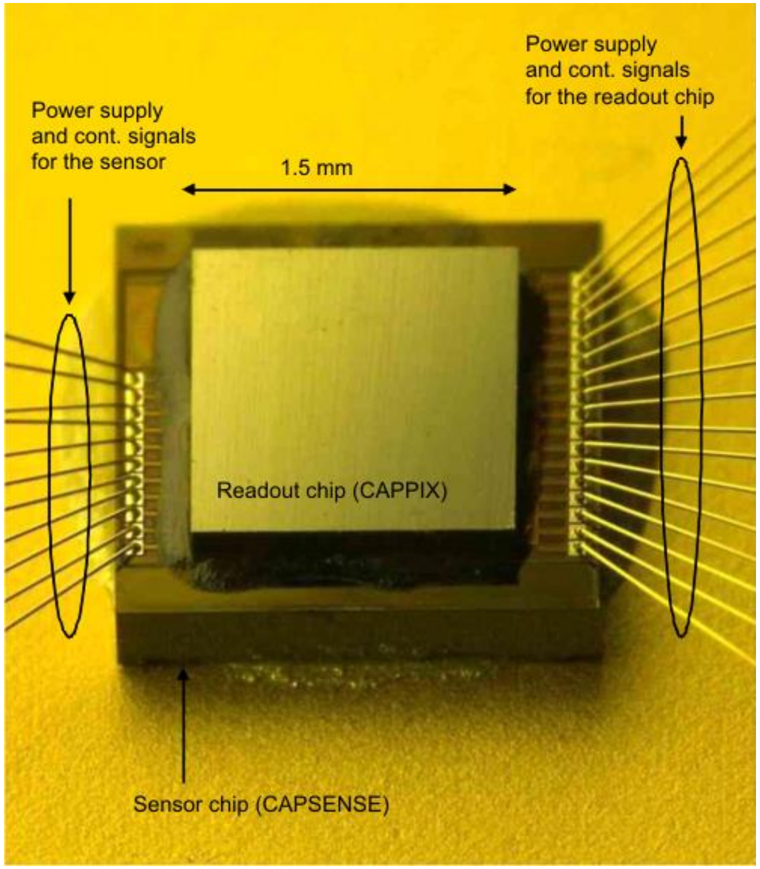
- ADC


Bricked pixels
Guard ring
21 um
213
Ramp
Switches
S/H Amplifier
S/H Amplifier
Difference Amplifier
Current source
Counter
Logic
Comparator
Difference amplifier
Pixels


Digitalblock
Pixel Matrix
IO Pads
Logik-Zelle (Standardzelle)

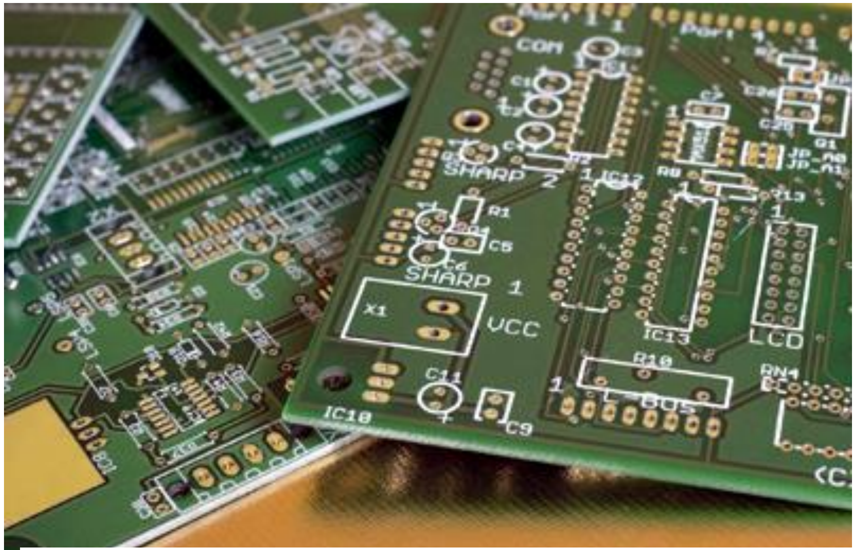
- IO Pads
- Drahtbonden
- ESD protection (ESD Schutz)



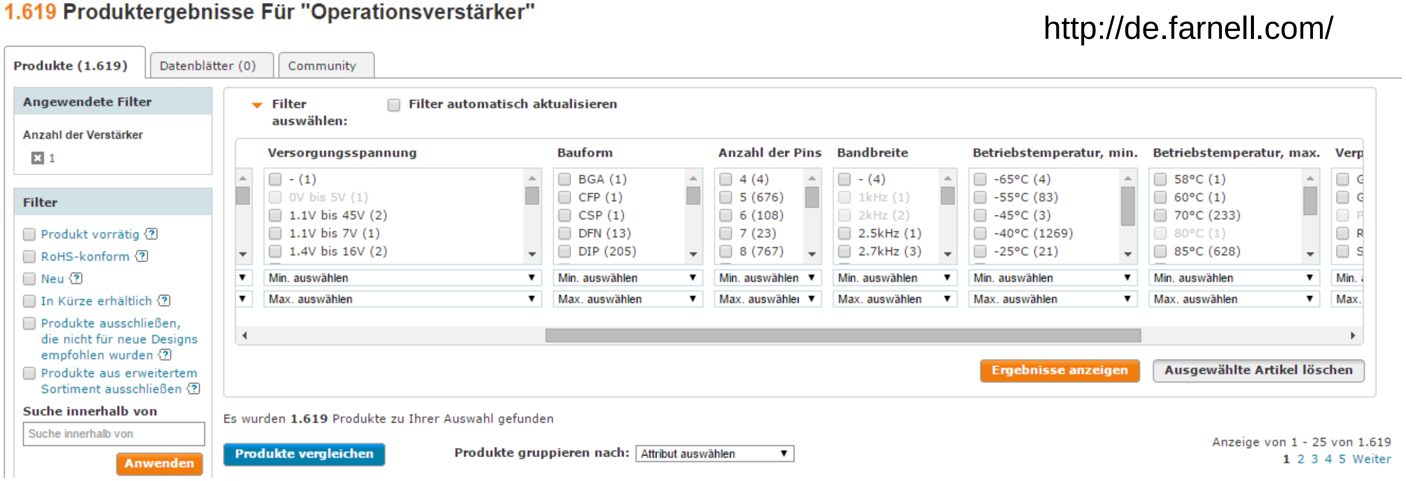

Power supply
and cont. signals
for the readout chip
Power supply
and cont. signals
for the sensor
1.5 mm
Readout chip (CAPPIX)
Sensor chip (CAPSENSE)

- Design analoger Schaltungen
- Techniken:
- Gegenkopplung
- AC, DC Analyse
- Stabilitätskriterien

- Leiterplatten-Design
- Viele kommerziellen Komponenten



http://www.pcb-pool.com/



1.619 Produktergebnisse Für "Operationsverstärker"

Produkte (1.619)
Datenblätter (0)
Community

Angewendete Filter

Anzahl der Verstärker
☒ 1

Filter

☐ Produkt vorrätig
☐ RoHS-konform
☐ Neu
☐ In Kürze erhältlich
☐ Produkte ausschließen, die nicht für neue Designs empfohlen wurden
☐ Produkte aus erweitertem Sortiment ausschließen

Suche innerhalb von

Suche innerhalb von

Anwenden

Filter auswählen: ☐ **Filter automatisch aktualisieren**

Versorgungsspannung	Bauform	Anzahl der Pins	Bandbreite	Betriebstemperatur, min.	Betriebstemperatur, max.	Verp
☐ - (1)	☐ BGA (1)	☐ 4 (4)	☐ - (4)	☐ -65°C (4)	☐ 58°C (1)	☐ G
☐ 0V bis 5V (1)	☐ CFP (1)	☐ 5 (676)	☐ 1kHz (1)	☐ -55°C (83)	☐ 60°C (1)	☐ G
☐ 1.1V bis 45V (2)	☐ CSP (1)	☐ 6 (108)	☐ 2kHz (2)	☐ -45°C (3)	☐ 70°C (233)	☐ P
☐ 1.1V bis 7V (1)	☐ DFN (13)	☐ 7 (23)	☐ 2.5kHz (1)	☐ -40°C (1269)	☐ 80°C (1)	☐ R
☐ 1.4V bis 16V (2)	☐ DIP (205)	☐ 8 (767)	☐ 2.7kHz (3)	☐ -25°C (21)	☐ 85°C (628)	☐ S
Min. auswählen	Min. auswählen	Min. auswählen	Min. auswählen	Min. auswählen	Min. auswählen	Min.
Max. auswählen	Max. auswählen	Max. auswähler	Max. auswählen	Max. auswählen	Max. auswählen	Max.

Ergebnisse anzeigen
Ausgewählte Artikel löschen

Es wurden **1.619** Produkte zu Ihrer Auswahl gefunden

Produkte vergleichen

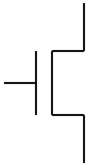
Produkte gruppieren nach: Attribut auswählen

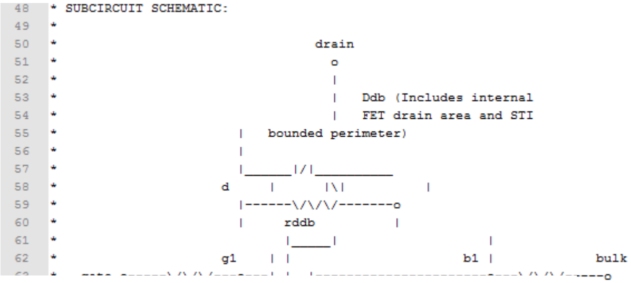
Anzeige von 1 - 25 von 1.619
1 2 3 4 5 Weiter

http://de.farnell.com/

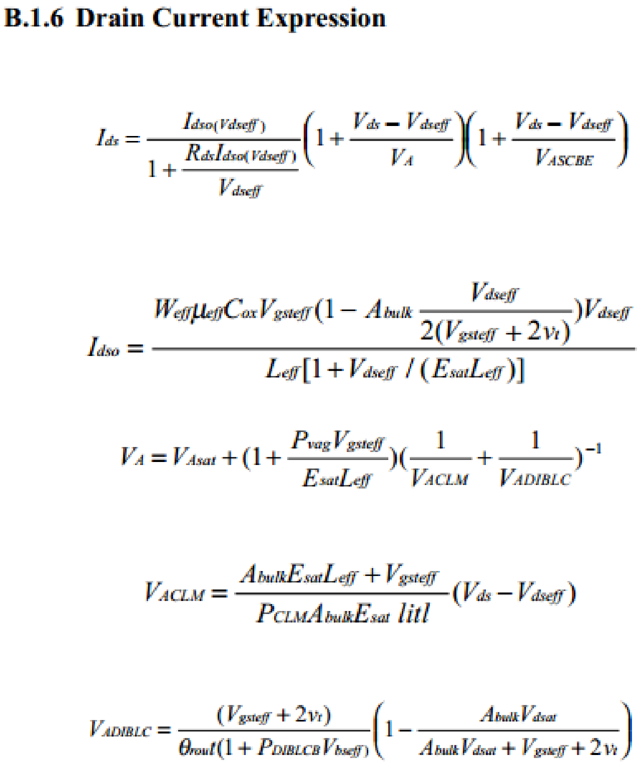
- IC-Design
- Nur zwei Grundkomponenten
- MOSFET als Verstärker, Stromquelle, Widerstand, Kondensator, Schalter, Diode verwendet
- Komplizierte MOSFET Modelle

- Komplizierte MOSFET Modelle





```
* SUBCIRCUIT SCHEMATIC:
*
*                               drain
*                                 o
*                                 |
*                                 |   Ddb (Includes internal
*                                 |   FET drain area and STI
*                     |   bounded perimeter)
*                     |
*                     |______|/|__________
*                   d     |      |\|         |
*                     |------\/\/\/-------o
*                     |     rddb          |
*                           |_____|              |
*                   g1    | |                 b1 |              bulk
```



B.1.6 Drain Current Expression

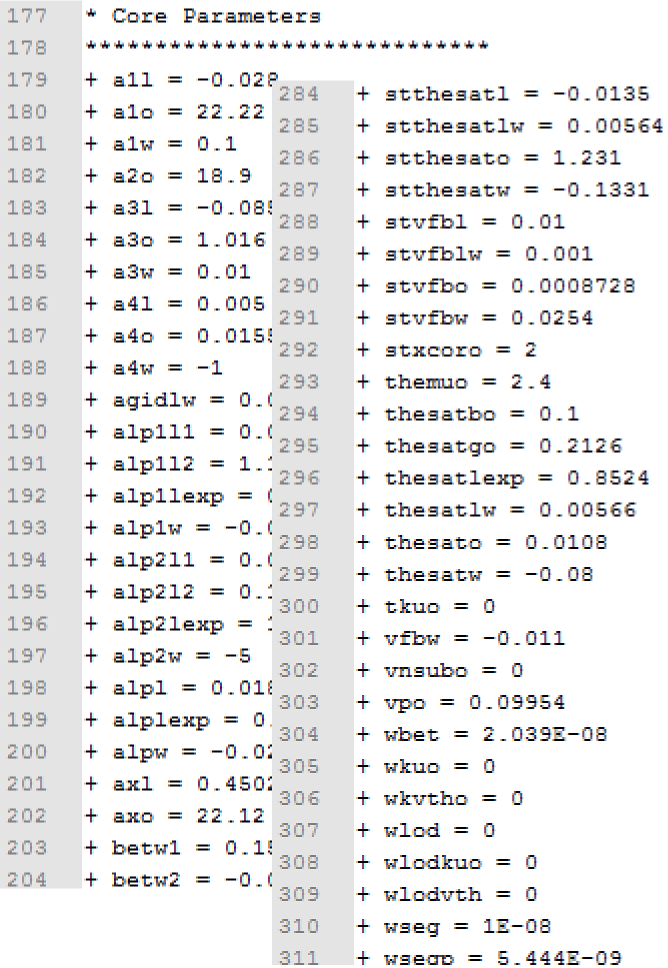
$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gsteff} (1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2v_t)}) V_{dseff}}{L_{eff}[1 + V_{dseff} / (E_{sat} L_{eff})]}$$

$$V_A = V_{Asat} + (1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1}$$

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat}\, \mathit{litl}} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + P_{DIBLCB} V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t}\right)$$



```
* Core Parameters
******************************
+ a1l = -0.02
+ a1o = 22.22
+ a1w = 0.1
+ a2o = 18.9
+ a3l = -0.08
+ a3o = 1.016
+ a3w = 0.01
+ a4l = 0.005
+ a4o = 0.015
+ a4w = -1
+ agidlw = 0.
+ alp1l1 = 0.
+ alp1l2 = 1.
+ alp1lexp =
+ alp1w = -0.
+ alp2l1 = 0.
+ alp2l2 = 0.
+ alp2lexp =
+ alp2w = -5
+ alpl = 0.01
+ alplexp = 0.
+ alpw = -0.0
+ axl = 0.450
+ axo = 22.12
+ betw1 = 0.1
+ betw2 = -0.
```

```
+ stthesatl = -0.0135
+ stthesatlw = 0.00564
+ stthesato = 1.231
+ stthesatw = -0.1331
+ stvfbl = 0.01
+ stvfblw = 0.001
+ stvfbo = 0.0008728
+ stvfbw = 0.0254
+ stxcoro = 2
+ themuo = 2.4
+ thesatbo = 0.1
+ thesatgo = 0.2126
+ thesatlexp = 0.8524
+ thesatlw = 0.00566
+ thesato = 0.0108
+ thesatw = -0.08
+ tkuo = 0
+ vfbw = -0.011
+ vnsubo = 0
+ vpo = 0.09954
+ wbet = 2.039E-08
+ wkuo = 0
+ wkvtho = 0
+ wlod = 0
+ wlodkuo = 0
+ wlodvth = 0
+ wseg = 1E-08
+ wsegp = 5.444E-09
```

- Widerstand und Diode selten benutzt
- Kondensatoren ersetzt Widerstände
- MOSFETs ersetzen Dioden
- Transkonduktor

- Inhalt des Kurses:
- Approximative Methode für Schaltungsanalyse
- Analyse von Schaltungen mit Rückkopplung
- Berechnung von Zeitkonstanten
- Stabilitätskriterien
- Verstärkern
- Komplexere Schaltungen
- Mehrstufige-, differenzielle-, Rail to Rail-Verstärkern, Komparatoren
- Systeme: Switched Capacitor Schaltungen, ADCs
- Jede zweite Woche Übungen mit Chipdesign-Software
- Prüfung – Mündliche Prüfung – Beispiele aus den Übungen

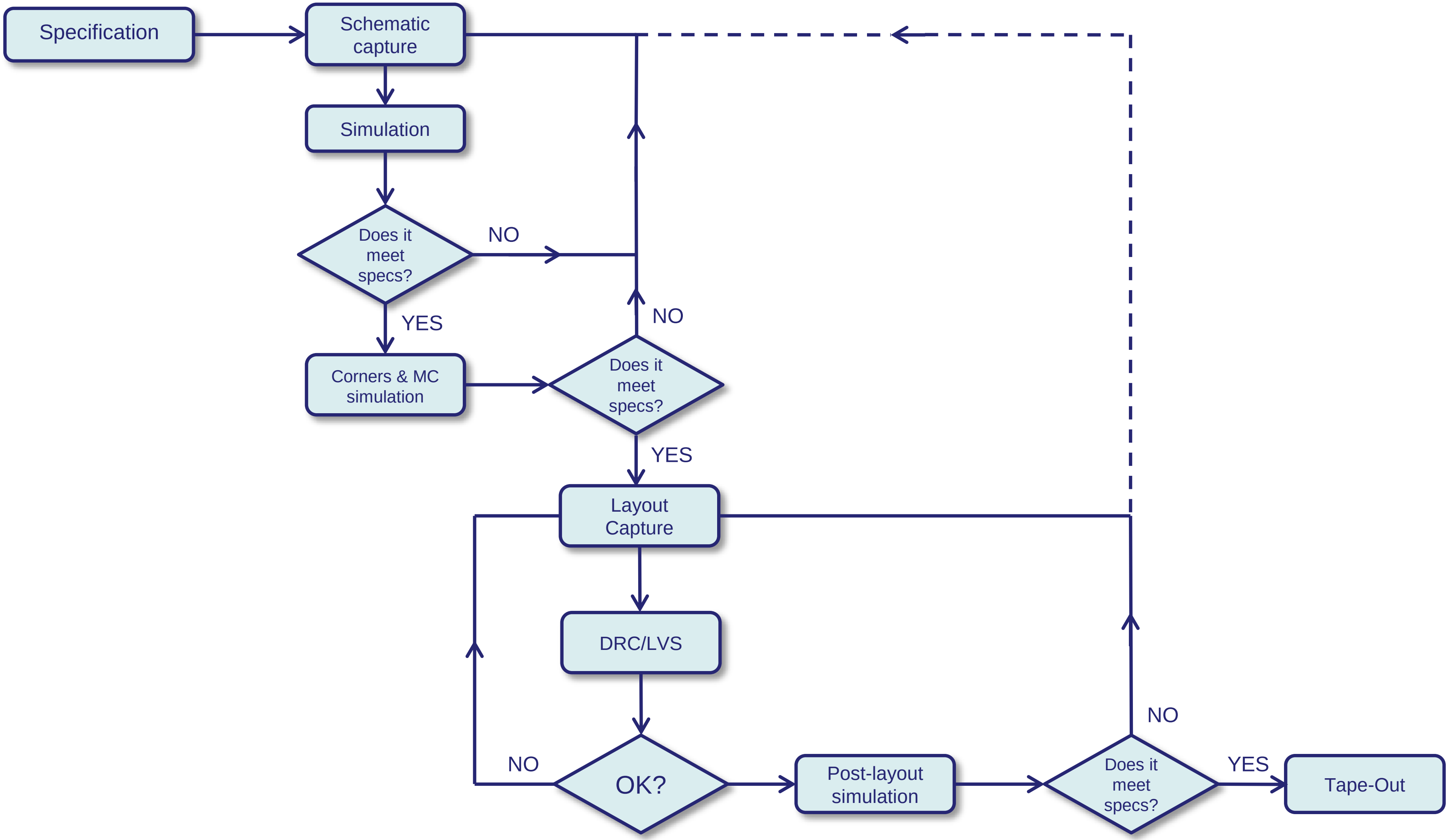
- Literatur
- **Design of Analog CMOS Integrated Circuits** von Behzad Razavi
- **Operation and Modeling of the MOS Transistor,** Yannis Tsividis, Colin McAndrew
- **Analog Integrated Circuit Design**, David A. Jones, Ken Martin, John Wiley & Sons, Inc
- **Analysis and Design of Analog Integrated Circuits**, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, Inc
- **The Art of Analog Layout**, Alan Hastings, Prentice Hall
- **CMOS Analog Circuit Design,** Allen-Holberg, Oxford Press, 1987
- **Analog Design Essentials,** W. Sansen, Kluwer International Series in Engineering and Computer Science
- **Microelectronics** von Jacob Millman von T (1999)

- Themen
- 1 Rückkopplung, Formeln für Schaltungen mit Rückkopplung, Einfluss auf Verstärkung, Zeitkonstanten, Invertierender und Nichtinvertierender Verstärker
- 2 Grundlegende Verstärker-Schaltungen und grundlegende Bauteile: CMOS Verstärker (Common Source), Cascode, Source-Folger
- 3 Halbleiter, Diode, MOSFET (DC, AC, Rauschen, Matching)
- 3ü Bipolar Transistor, MOS-Kondensator, Schwache Inversion, BSIM-Modell
- 4 AC Analyse (Frequenzverhalten der Schaltungen), Übertragungsfunktion für Schaltungen mit Kondensatoren, Bestimmung von dominanten Zeitkonstanten (RC Regel), Methode der Nullimpedanzen
- 4ü Common Source Verstärker
- 4ü Single Ended Verstärker, Kaskaden und Kaskoden
- 5 Einfluss von Rückkopplung auf Zeitkonstanten, Stabilität, Nyquist Regel
- 5ü Transimpedanz Verstärker, Spannungsregler
- 7 Komplexere Verstärker, Einstufig, Zweistufig, Rail to Rail, Volldifferentiell, Klasse AB
- 8 Komparatoren
- 9 Switched Capacitor Schaltungen
- 10 Filter (RC, Gm-C, Switched Capacitive Filter)
- 11 ADCs (Dual und Single Slope, Flash, Subranging, SAR mit Kondensatoren, SAR mit Stromquellen, SAR Asynchron, Sigma Delta, Zyklisch mit Stromzellen, Zyklisch mit Switched Capacitive Schaltungen)
- 12 Spannungsreferenz, PLL und VCO, LVDS Treiber, LVDS Empfänger

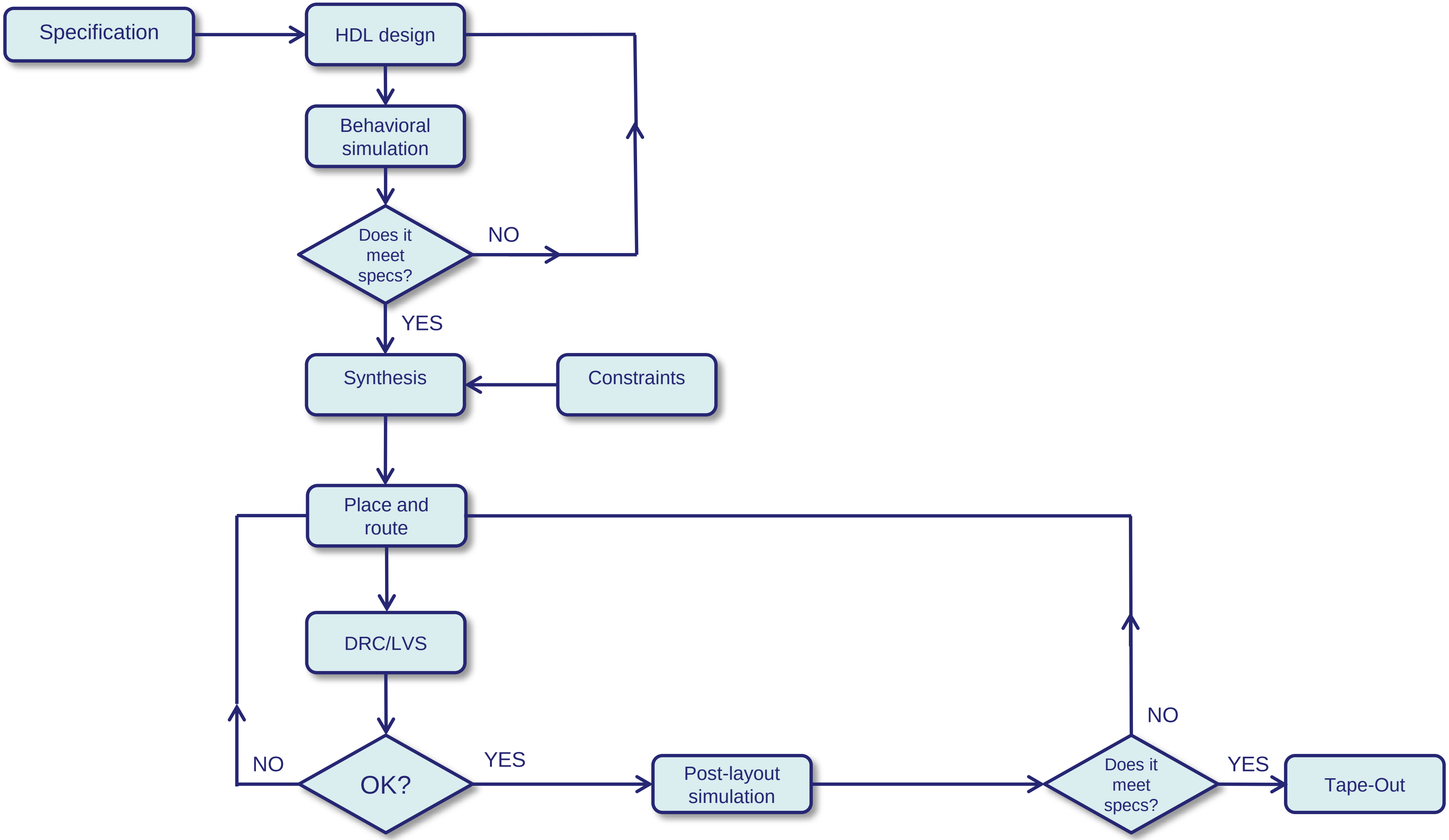
- Was haben wir gelernt?
- Es geht um analoges Chipdesign
- Chipdesignsoftware Cadence – Übungen
- Analoges Designflow: Schaltungsentwurf, Simulation (AC, DC, Transiente Simulation, Rauschen, Matching), Layoutentwurf, DRC, LVS
- Digitales Designflow: HDL Code, Simulation -> (automatische) RTL Synthese, Simulation (Standard-Logikzellen) -> Layout-Synthese, Simulation
- Am Anfang des Projekts muss man Hersteller (foundry, vendor) und Technologie wählen, PDK (Process Design Kit) (Technologiespezifische Bibliotheken fürs Cadence) besorgen
- Europractice
- Transistorherstellung siehe Link
- Chipprojekte sind hierarchisch aufgebaut
- Grundbausteine: Common Source, Cascode, Source Follower, Current Mirror, Differenzpaar
- Widerstände selten benutzt – Alternative ist C
- Transistormodelle sind sehr komplex – BSIM Model
- Fragen
- Welche Chiphersteller kennen wir?
- AMS, TSMC, UMC, IBM, GF, LF, XFAB…
- Welche Prozesse?
- CMOS, SOI, HVCMOS, FINFET, BCD, BiCMOS
- Welche „process nodes“: 0.35, 0.24, 0.18, 0.13, 90nm, 65nm, 45nm…
- Das meistbenutzte MOSFET-Modell: BSIM
- Welche Firmen sind fürs Leiterplattendesign nützlich? PCB pool, Farnel

- Vielen Dank für Ihre Aufmerksamkeit

Analog Design Flow


Specification
Schematic capture
Simulation
Does it meet specs?
NO
YES
Corners & MC simulation
NO
Does it meet specs?
YES
Layout Capture
DRC/LVS
NO
OK?
Post-layout simulation
NO
Does it meet specs?
YES
Tape-Out

Digital Design Flow


Specification
HDL design
Behavioral simulation
Does it meet specs?
NO
YES
Synthesis
Constraints
Place and route
DRC/LVS
NO
OK?
YES
Post-layout simulation
NO
Does it meet specs?
YES
Tape-Out